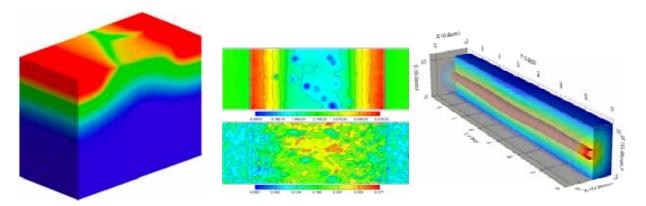
SIMULATION OF ATOMIC SCALE STATISTICAL VARIABILITY IN NANO-CMOS DEVICES USING DD, MC AND QT SIMULATION TECHNIQUES

Asen Asenov **Device Modelling Group** Department of Electronics and electrical Engineering The University of Glasgow

Intrinsic parameter fluctuations associated with discreteness of charge and granularity of matter are now a major factor limiting scaling and integration [1]. The accurate modelling and simulation of such effects is a very important for the development of the present and next generations nano-CMOS device and their integration of giga-transistor count chips. We will present recent advances made by the Glasgow Device Modeling Group in the simulations of intrinsic parameter fluctuations using Drift Diffusion (DD), Monte Carlo (MC) and Quantum Transport (QT) techniques. Examples include:



potential pinning at poly-Si current distribution obtagrain boundaries in the surfa- ined from 3D MC simulace potential in the channel of tion featuring 'ab initio' 30x30nm MOSFET.

ionized impurity scattering.

Fig. 1 Impact of the surface Fig. 2 Surface potential and Fig. 3 3D NEGF current density contours in a 6nm nanowire MOSFET subject to interface roughness

- The resolution of discrete dopants in DD simulations [2] and the impact of the surface potential pinning and the doping nonuniformity at the poly-Si grain boundaries on the threshold voltage fluctuations in conventional bulk MOSFETs (Fig. 1).
- The development of 3D Monte Carlo device simulator featuring ab-initio ionised impurity and quantum confinement scattering. The impact of ionised impurity scattering on current fluctuations in bulk MOSFETs. The impact of quantum confinement scattering on current fluctuations in double gate MOSFETs [3] (Fig. 2).
- The development of the first fully 3D real space NEGF simulator. The impact of interface roughness and stray charges on the current variations in nanowire transistors (Fig.3).

References

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- [3] C. Riddet et al., IEEE Trans. Nanotechnol. 6 48 (2007)