SIMULATION OF THE GATE LEAKAGE CURRENT IN SURROUNDING GATE (SG) MOSFETS BASED ON AN ANALYTIC POTENTIAL MODEL

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Over the past three decades, the exponential growth of the microelectronics industry has been enabled primarily by continuous scaling of dimension reduction of metal-oxide-semiconductor field-effect transistor (MOSFET). The inherent benefits of MOSFET scaling are the speed improvement and energy reduction associated with a binary-logic transition. Various device structures such as double gate fully depleted SOI, triple-gate and gate-all-around structures hence, have been extensively studied to restrict short-channel effects (SCEs) within a limit while achieving the primary advantages of scaling, i.e. higher performance, lower power, and ever increasing integration density [1,2]. Among these devices SG-MOSFET, illustrated in Figure 1, have recently drawn wide research interest due to their excellent SCEs immunity compared to other contemporary device structures [3]. Several physical limiting factors associated with the ultrathin gate oxides have been identified, including direct tunneling currents [4]-[5], polysilicon depletion effects [6], and oxide reliability [7]. Among them, the direct tunneling is the most sensitive one to the oxide thickness and it plays a significant role in a SG-MOSFET because is a source of parasitic current and contribute to the stand-by power consumption of integrated circuits. Many papers on modelling the tunneling current in the MOS system consider the tunnel current under equilibrium ($V_{ds} = 0$). However, if the equilibrium is broken ($V_{ds} \neq 0$) the distribution of the potential energy and the quasi Fermi level changes along the channel and calculation of the gate tunnel current requires taking into account this effect. In this study we use analytic physics based expressions for the potential energy and Fermi level of the SG MOSFET [8], which depends on the position through the channel. To account for the quantum effects we solve the Schrödinger equation for correcting the classical surface potential [9]. The direct tunneling current is calculated by means of three fundamentals parameters: i) the transmission probability, calculated with a modified WKB approximation and taking into account the reflections from all boundaries within of the oxide, ii) the frequency f at which the electrons tunnel through the gate oxide, iii) the inversion charge density, which depends on 1-D density of states and Fermi-Dirac statistic [10]. The main result is the comparison between classical and quantum models for direct tunneling current and the leakage current dependence on the source-drain voltage, gate-source voltage and thickness of the silicon. Besides we show the differences between gate tunneling current results obtained with the commercial DESSIS^{TM} simulator and our model.

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Figures:

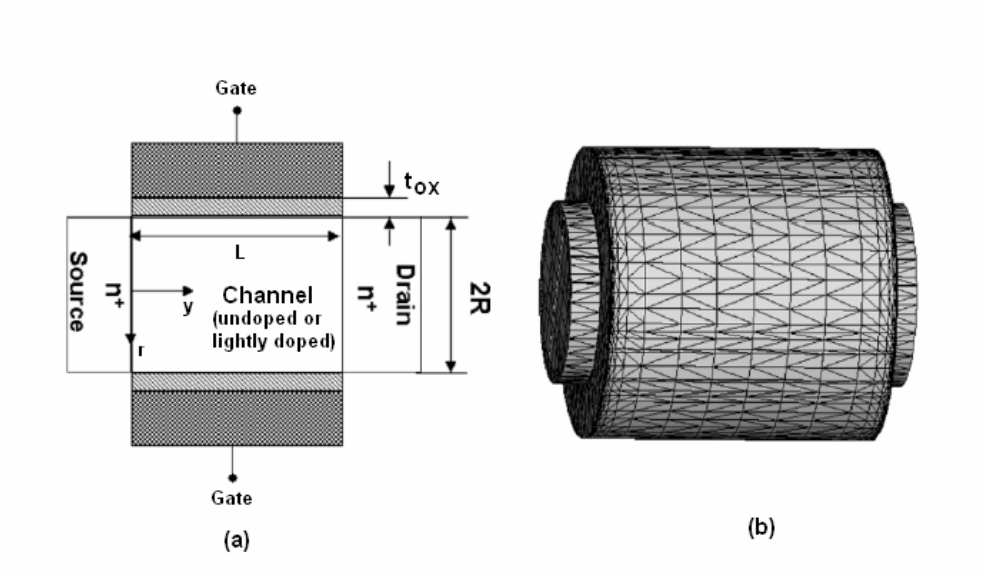

Fig. 1. (a) Cross section of the SG-MOSFET. (b) Simulated geometry of the SG-MOSFET using ISE-TCAD^{TM}.