Poster

CARBON NANOTUBE BASED INTERCONNECTS

Jean-Christophe Coiffic[1], H. Le Poche[2] , M. Fayolle[1], S. Maîtrejean[1], G.Passemard[1]
[1]CEA LETI D2NT/LBE 17, av. des Martyrs 38054 GRENOBLE Cedex9 France
[2]CEA LITEN DTNM/LCH 17, avenue des Martyrs 38054 GRENOBLE Cedex9 France
+33438785311
jean-christophe.coiffic@cea.fr

Achieving always faster and smaller devices implies new challenges. The whole wiring scheme (fig.a) used to interconnect different transistors in chips is highly sensitive to scale reduction and, in the following decade years, the microelectronic industries will be faced with insurmountable issues [1]. Indeed interconnect RC delay, crosstalk and power consumption increase. Moreover current densities and heat dissipation are becoming critical points which largely affect interconnections reliability. A solution could be the use of carbon nanotube (CNT) [2-3] instead of traditional copper vertical interconnects called vias. Our work is focused on integrating CNT as metallic wires for ULSI on 200mm diameter wafers with standard microelectronic industry requirements. Main issues are thermal budget limitation and selective CNT growth in the bottom of high aspect ratio vias holes on copper line.

For this study, a new highly conductive diffusion barrier between copper and catalyst has been developed. After catalyst localization, a low thermal CVD (520°C) method is then employed to grow multiwall nanotubes. The process has been engineered to grow nanotubes on 300 cm2 substrates in a single run, showing the industrial scalability of such parallel method. Via holes down to 140nm wide have been realized. CNTs grown are multiwalls and a high density of 5.10^10 CNT/cm2 per via is obtained (fig.c). After depositing and patterning AuPd contacts, electrical measurements are performed. First measurements (fig.d) on 300nm wide CNTs vias show ohmic behaviour at low voltage (<2V) with low resistance of 80Ω. By increasing voltage, current follows a power law. Interestingly, resistance decreases as voltage increases. This behaviour could be the result of inner shell transport enhancement.

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References:

[1] International technology roadmap for semiconductors http://public.itrs.net/
[2] F. Kreupl, IEDM Tech. Dig., pp. 683 - 686, December 2004
[3] M. Nihei, M. Horibe, Japan, IITC 2006

Figures:

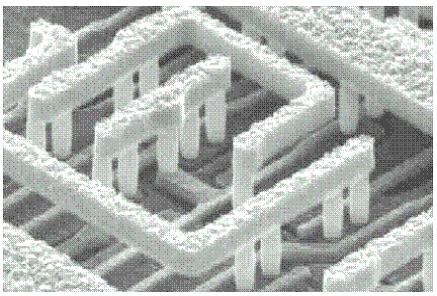

Fig.a: Copper interconnections (lines [horizontal] and vias [vertical]) in a chip after removing the dielectric filling.

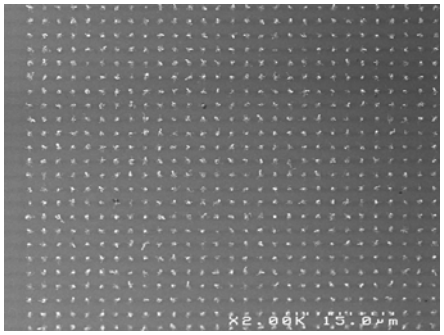

Fig.b: SEM view of an array of CNTs filled vias (top view)

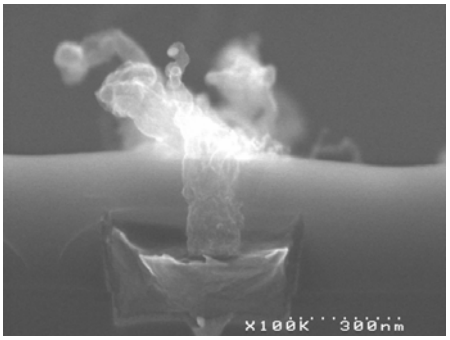

Fig.c: SEM cross section of a 140nm wide via on a copper line. Surrounding dielectric is silicon dioxide. Nanotube density is $5.10^{\wedge 10}$ CNT/cm^2 per via.

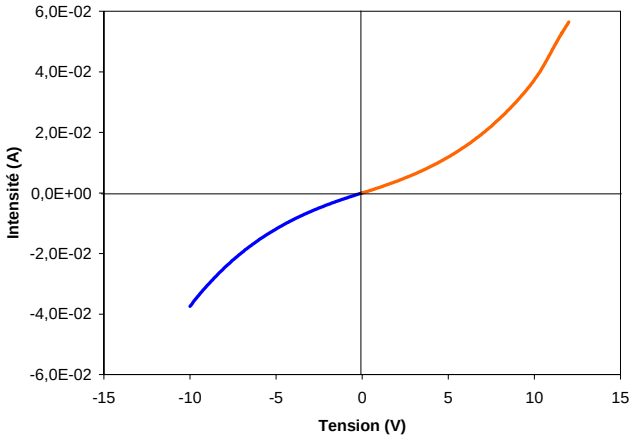

Fig.d: Electrical characteristic of a 300nm wide via. Low voltage show ohmic behaviour and for a higher voltage current follows a power law.