# MODELING OF ELECTRONIC AND TRANSPORT PROPERTIES OF SEMICONDUCTOR NANOWIRES

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Semiconductor nanowires have emerged as promising building blocks for nano- and opto-electronic devices. The physics of nanowires has proven to be both rich and complex contributing with both new physics and promising device properties. However, to properly understand and take advantage of the characteristics of the nanowire it is often helpful to do theory and modeling on the nanowire system. In this talk we will show examples of strain, doping and charge transport modeling in semiconductor nanowires.

It is well known that freestanding nanowires allows for a larger lattice mismatch compared to 2D systems. We have studied an InAs/InP nanowires with both longitudinal and lateral heterostructure analyzing the strain distributions as well as the piezoelectric potential.[1] We will show how the strain relaxes towards the surface of the nanowire and that the strain will create a significant barrier lowering between InAs and InP in short InP barriers and InAs quantum dots.

An important issue for many nanowire devices is the ability to introduce effective doping inside the nanowire. We have studied the effect of the dielectric environment on the dopant binding energies.[2] The binding energy is found to increase with decreasing nanowire radius. Already at R=10 nm the effect is large enough to seriously hinder the thermal excitation of the dopant electrons. We will also show that by changing the dielectric surrounding of the nanowire, i.e. the addition of a shell or an all around gate, the increase in binding energy can be reduced allowing for effective doping of small nanowires.

Silicon nanowires are considered as promising candidates for transistor downscaling since they can be manufactured with small radius ($R \approx 1$nm) and since they allow for “all around gates”, which improves the gate efficiency compared to the classical planar technology. However, as the nanowire channel is scaled down effects from surface disorder will become important. We have studied the effect of surface roughness disorder on the intrinsic properties of the silicon nanowires.[3] Due to the band structure anisotropy of silicon the study have been carried out for three different nanowire orientations, [100], [110] and [111]. We will show that the [110] and [111] orientations have the best mobility for electrons and holes respectively. We will also show that our findings can be explained by the anisotropy of silicon and thus that the conclusions drawn for our particular surface roughness model likely holds for other kinds of disorder, e.g. trapped charges.

**References:**

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