FERROELECTRIC MATERIALS TO THE AID OF LOW-POWER SWITCHING

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One of the most severe problems in the field of microelectronics is the evacuation of heat dissipated during data processing [1]. Although a single semiconductor device produces a tiny amount of heat (around 10^{-16} J), integrated circuits today contain about 10^9 devices. The problem has led to a power crisis in manufacturing of semiconductor devices, which could well end up with Moore's law. To achieve the integration of 10^{12} devices, which would enable new features not yet imagined, and a significant reduction of integration cost, some radical new solution that allows handle the problem of heat dissipation is required. One possibility is to dissipate less power (P_{active}) during transistor switching. The most effective way to reduce power is to reduce the supply voltage (V_{dd}), as $P_{active} \propto CV_{dd}^2 f$ (where C is the total equivalent capacitance to be charged and discharged in a clock cycle, and f is the frequency of the clock). For high-performance digital applications –e.g, microprocessors for personal computers- reducing V_{dd} must be accompanied by a reduction of the threshold voltage (V_{th}), for not to worse the delay time. However, reducing V_{th} implies an exponential increase of dissipated power in the OFF state (P_{off}). Accordingly, downscaling of V_{dd} can not be applied without limit as a strategy to reduce power consumption, as P_{off} would grow uncontrollably. The reason is that the subthreshold slope (a figure of merit that describes the goodness of the transition OFF-ON/ON-OFF) of a conventional transistor is not scalable and presents a fundamental thermodynamic limit of S=60 mV/decade at room temperature. This limit is known as the *Boltzmann tyranny* and is widely accepted by the scientific community that is not possible to obtain S<60 mV/decade without changing the principle of operation of the transistor.

In this project I will explore a change in the design of conventional transistor in order to achieve subthreshold slopes below 60 mV/decade. The proposal is replacing the conventional gate insulator (a dielectric material) with a ferroelectric material [2-4]. This type of material presents a region of negative capacitance in its Q-V curve (charge vs. applied voltage) (Figure 1a). A negative capacitance means that by increasing the applied voltage then the stored charge decreases. This region of negative capacitance is not directly observable in experiments but, if the ferroelectric material is associated in series with a small enough capacitance, the conditions for its observation should be fulfilled. The role of this capacitance is played by the channel-substrate capacitance. The negative capacitance provides a mechanism for amplifying the surface potential (Figure 1b). The gain (G) could be around 4, although this limit is an issue that should be further explored. The amplification of the surface potential is the key ingredient for increasing the current in more than one order of magnitude for every 60 mV increase in gate voltage (Figure 1c).

[1] *International Technology Roadmap for Semiconductors. Available: public.itrs.net*
[2] S. Salahuddin and S. Datta, *Nano Letters* **2008**, no. 2, 405-410.
[3] J. F. Scott and C. A. Paz de Araujo, *Science* **1989**, 246, 1400-1405.
[4] J. F. Scott, *Science* **2007**, 315, 954-959.

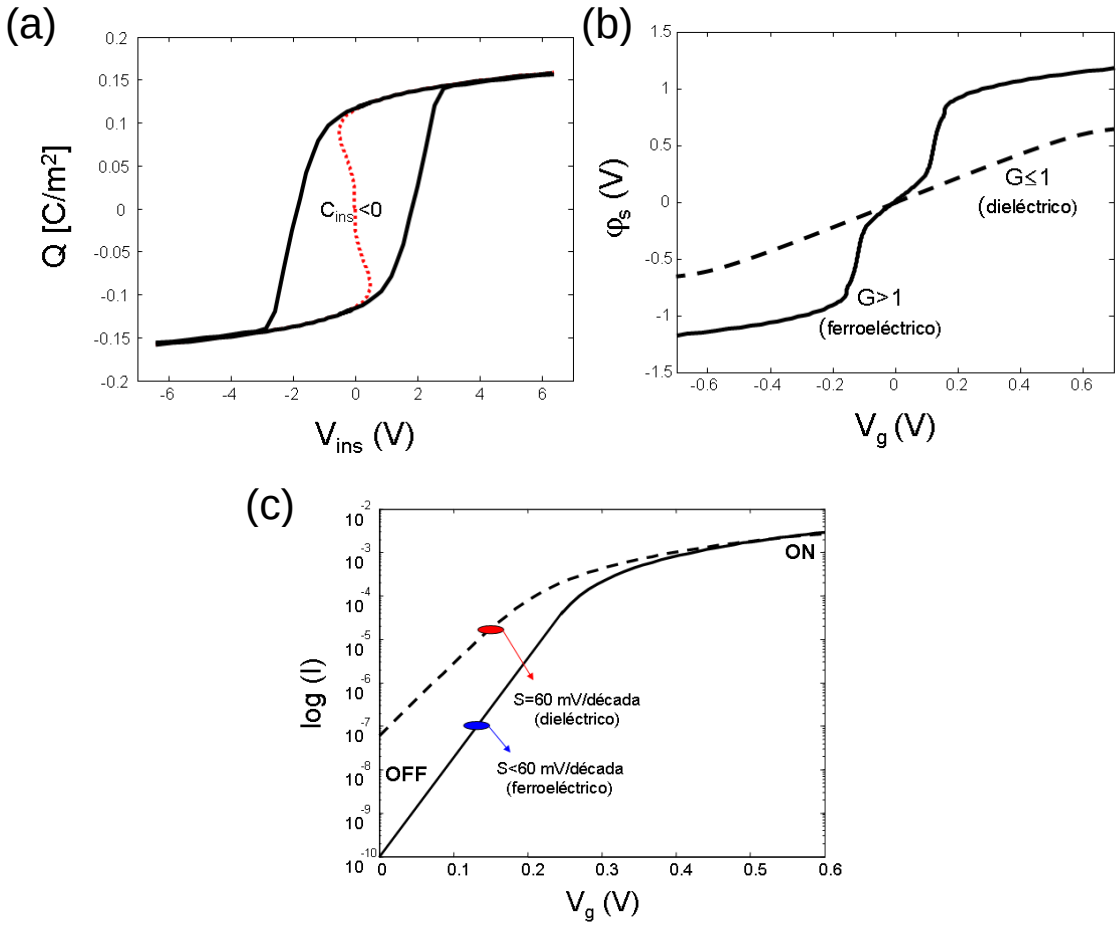

Figure 1. (a) Stored charge (Q) vs applied voltage (V_{ins}) for a typical ferroelectric material. Dashed line shows the **negative capacitance region** (C_{ins}<0). (b) Dielectric insulators exhibit positive capacitance (C_{ins}>0) and the surface potential (φ_s) follows the gate voltage (V_g) with a gain G ≤1 (dashed line). Ferroelectric insulators, operated in the negative capacitance region, could result in surface potential amplification (G>1) (solid line). (c) A gain G=1, which is the maximum gain with a dielectric insulator, results in a subthreshold slope S=60 mV/decade (dashed line). If we replace the insulator by a ferroelectric material operated in the negative capacitance region, then G>1 and S<60 mV/decade (solid line).