RACETRACK MEMORY: A STORAGE CLASS MEMORY BASED ON CURRENT CONTROLLED MAGNETIC DOMAIN WALL MOTION

Stuart Parkin
IBM Research Division, Almaden Research Center, San Jose, California, USA
Phone: +1 (408) 927 2390; email: parkin@almaden.ibm.com

Racetrack Memory promises a novel storage-class memory with the low cost per bit of magnetic disk drives but the high performance and reliability of conventional solid state memories(*1*). Unlike conventional memories, the fundamental concept of Racetrack Memory (RM) is to store multiple data bits - as many as 10 to 100 bits- per access point, rather than the typical single bit per transistor. This is accomplished in Racetrack Memory by storing data bits in the form of domain walls in magnetic nanowires which are oriented either parallel to the surface or perpendicular to the surface of a silicon wafer (see Figure 1). These distinct structures form "horizontal" and "vertical" Racetrack Memories. Conventional CMOS devices and circuits are used to provide for the creation and manipulation of the domain walls in the magnetic nanowires or "racetracks". The domain walls are shifted along the nanowires using nano-second long current pulses via the transfer of spin angular momentum from the spin polarized current generated in the magnetic nanowire racetracks(*2*).

In this talk we discuss progress towards building a Racetrack Memory and the fundamental physics underlying it. In particular, we discuss the current and field controlled dynamical motion of magnetic domain walls in magnetic nanowires formed from permalloy and related materials.

The structure of domain walls in sufficiently narrow permalloy nanowires are either of transverse or vortex types. These walls display two chiralities, clockwise and anti-clockwise, which have equal energies in smooth nanowires. In addition, the vortex walls have a tiny core region with an out-of-plane magnetization which consequently has a polarity (up or down). The transverse and vortex wall structure and the number of domain walls can be determined from the anisotropic magnetoresistance displayed by permalloy(*3*). By introducing pinning sites in the nanowire the chirality can also be determined(*3*). The polarity of the core of the vortex domain walls can be inferred from the resonant ac current excitation of a trapped domain wall(*4*).

The current and field induced motion of domain walls along permalloy nanowires is distinctly different in smooth nanowires versus those which have intrinsic or extrinsic pinning sites. We discuss the resonant excitation of pinned domain walls by using a succession of current pulses whose temporal length and separation are tuned to the fundamental harmonic frequency of the domain wall arising from its being trapped in a local pinning potential(*5-6*).

The field driven dynamical motion of domain walls is complex. In small magnetic fields the structure of the domain walls is unchanged during their motion but, above a certain threshold field, which is distinct for transverse and vortex walls, the domain wall structure oscillates periodically between transverse wall structures of different chiralities and vortex and anti-vortex wall states(*7-8*). By using spin-valve nanowire structures the stochastic dynamical behavior of the current and field driven motion of the domain walls can be observed. The stochasticity has a complex field dependence and is greatest for intermediate field values(*9*).

Finally, we discuss the development and demonstration of a current-controlled domain wall shift register(*10*). We discuss recent studies in which up to six domain walls can be injected and moved with the same current pulse along permalloy nanowires.

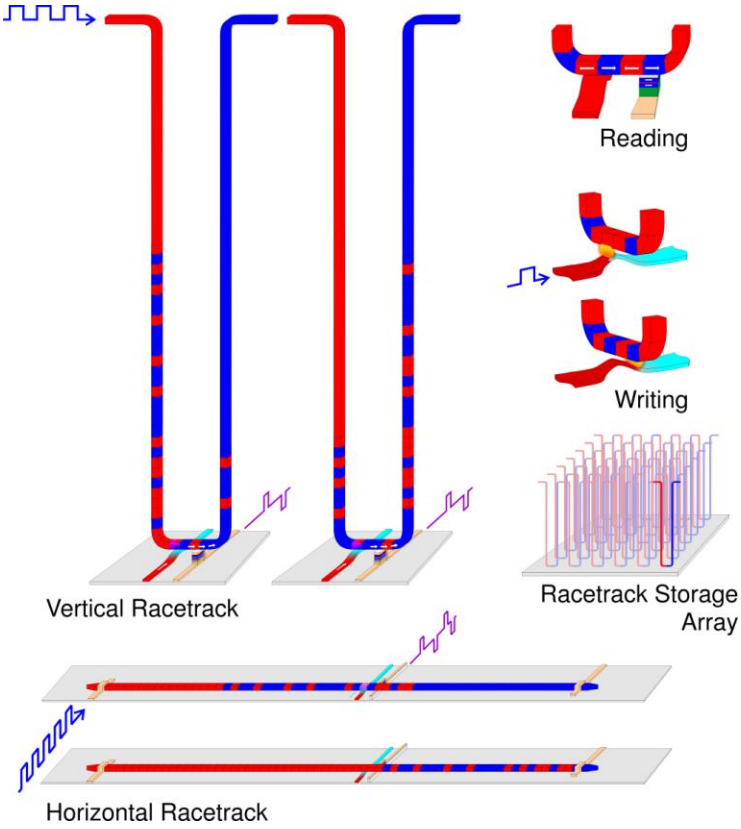

Figure 1: The Racetrack Memory is a novel innately three-dimensional memory device in which many data bits are stored per access element. In the vertical racetrack tall columns of magnetic material are arranged above the surface of a silicon wafer. Conventional silicon based microcircuits are fabricated within the silicon wafer to provide the electronic devices needed to operate the memory. The data is stored in the Racetrack in the form of magnetic domain walls. These domain walls separate magnetic regions which are magnetized in opposite directions (which can be parallel or perpendicular to the nanowire's direction). The domain walls are written into the Racetrack using one writing device per Racetrack. As illustrated a possible writing element is formed by moving a single domain wall along a neighboring wire. The magnetic fringing fields from the domain wall writing element can be used to write domain walls into the Racetrack. All the domain walls in the Racetrack are shifted along the Racetrack in lockstep by short pulses of spin-polarized current. The domain walls are read by moving them to a reading device - one per racetrack. The reading device can be formed from a magnetic tunnel junction magnetoresistive sensing element. By arranging many vertical Racetracks per unit area very high storage densities are possible, comparable to those of magnetic hard disk drives. However, the Racetrack Memory has no wear-out mechanism and is thus highly reliable. A second form of Racetrack Memory is one in which the Racetracks are placed horizontally on the surface of the silicon wafer. This type of memory is much easier to fabricate. The density of the nanowires is reduced, however, so that the storage capacity will be less than a hard disk drive but rather comparable to FLASH memory. This Racetrack Memory has much higher performance than FLASH, has no wear-out mechanism and uses much less energy.

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