Massive fabrication of Single-Walled Carbon Nanotube Field Effect Transistors

I. Martin-Fernandez [a], *M. Sansa* [a], *M.J. Esplandiu* [b], *F. Perez-Murano* [a], *E. Lora-Tamayo* [a], *P.Godignon* [a]

[a] *Insto. de Microelectrónica de Barcelona (IMB-CNM-CSIC), Campus UAB, Cerdanyola del Vallès, Spain.*
[b] *Departamento de Química, Universidad Autónoma de Barcelona (UAB), Campus UAB, Cerdanyola del Vallès, SPAIN.*

inigo.martin@imb-cnm.csic.es

First field effect transistors (FET) based on individual carbon nanotubes (CNTs) were fabricated in 1998 [1,2]. Since then, different strategies have been proposed to overcome the main challenges to achieve batch, high throughput and massive fabrication of these devices, among them, gaining control over the chiral vector and over the growth direction of the nanotube, which still remain subjects of research.

We present a process for massive fabrication of back-gated SWCNT-FET structures at wafer scale. This technology provides a platform to obtain a very high number of structures (~140,000 per 4 inch wafer) for statistical analysis of CNT-FET electrical and physical characteristics. In addition, it can enable the production of CNT-FET based sensors at an affordable cost.

The technological process is composed of 15 CMOS compatible microfabrication steps. The definition of the devices is accomplished by photolithography, instead of using electron beam lithography as in previous works [3]. Main steps of the process are summed up in Figure 1. CNT catalyst consists in a $Fe/Mo/Al_2O_3$ solution that is spin coated and then patterned by a lift-off process. CNT synthesis takes place in a rapid thermal CVD system at 800ºC using CH_4 and H_2. Catalyst deposition and growth conditions are optimized in order to have very few, one or zero SWCNTs being contacted by drain and source. As usual, metallic and semiconducting CNTs are randomly obtained.

A photograph of a 100 mm diameter wafer containing thousands of functional SWCNT-FET devices is shown in Figure 2(a). Optical microscope images in (b) show the high density of structures forming one of the chips and magnification of one of the different contact metals designs. AFM image in (c) shows one SWCNT-FET device with one SWCNT being contacted by both source and drain electrodes. The gap is 0.7 microns in this case.

An automatic probe system is used to obtain the electronic characteristic of the devices in a two step procedure (Figure 3). First, drain-source (I_{DS}) electrical current at every CNT-FET structure is measured for V_G=-5V and V_{DS}=0.3V. Then, a computational selection of devices is done to distinguish short circuit, open circuit, operative transistors and contacted metallic SWCNTs. In this way, the impact of the geometrical and process parameters can be evaluated. Based on this selection, individual I_{DS}/V_{GS} measurements for different values of V_{DS} are performed in the pre-selected transistors.

In conclusion, we present a technological process and a characterization procedure for massive fabrication and characterization of semiconducting SWCNT-FET structures. The platform is now being used for experiments on electric characterization of SWCNTs and the technology can also be applied to the fabrication of SWCNT based NEMS and sensors.

References:

[1] R. Martel, T. Schmidt, H.R. Shea, T. Hertel, and P. Avouris, Applied Physics Letters, **73** (1998), 2447-2449.

[2] S.J. Tans, A.R.M. Verschueren, and C. Dekker, Nature, **393** (1998), 49-52.

[3] G. Rius, I. Martin, P. Godignon, A. Bachtold, J. Bausells, E. Lora-Tamayo, and F. Perez-Murano, Microelectronic Engineering, **84** (2007), 1596-1600.

Figures:

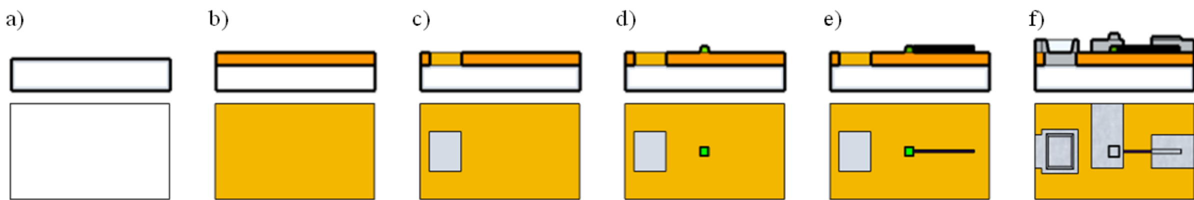

Figure 1: Technological process: a) P doped Si substrate; b) thermal oxidation of Si; c) selective dry etching of the SiO_2 layer; d) selective deposition of the catalyst material; e) CVD synthesis of SWCNTs; f) patterning, deposition and lift-off of the metal layer.

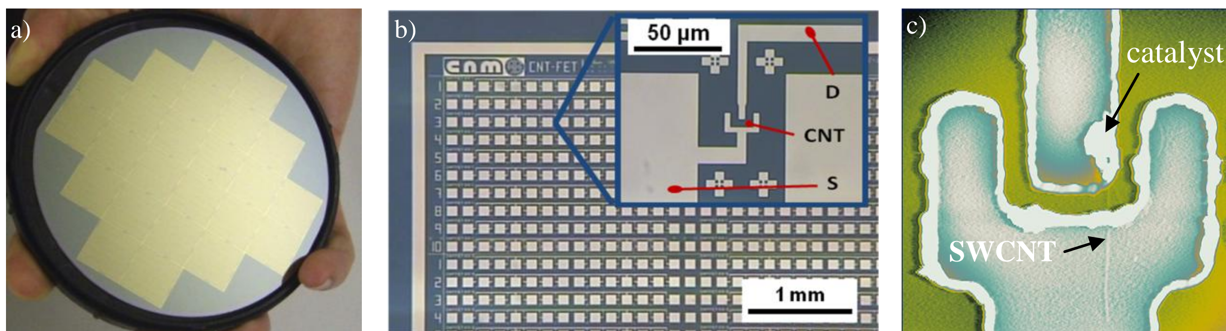

Figure 2: a) 4 inch SWCNT-FET wafer; b) details of one of the twenty four chips on the wafer and one of the CNT-FET structures; c) 10 x 10 µm^2 AFM image of one functional SWCNT-FET structure.

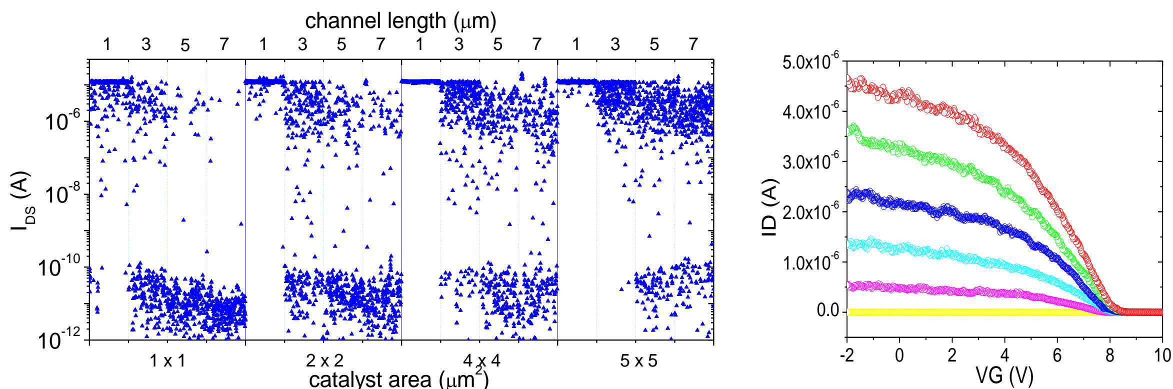

Figure 3: Electrical characterization of the devices. a) Automatically obtained "map" of one of the chips containing 5,760 structures. The impact of the catalyst deposition area and of the gap between source and drain on the number of working transistors is observed. After examining the data, individual measurements are performed only on devices showing a semiconducting characteristic (b).