CARBON NANOTUBE PROGRAMMABLE DEVICES FOR ADAPTIVE ARCHITECTURES

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Nano-objects with well defined structures and original electronic properties are of great interest for the development of new generation circuits. Their intrinsic nanometer scale, potentially associated with novel functionalities, is particularly interesting to complement CMOS. However, it is very unlikely that conventional architectures developed so far for the CMOS technology will be ideally suited for these new objects. These architectures can barely cope with any significant variation in either electrical characteristics or placement of individual devices, which are an inherent particularity of most nano-devices. On the other side, adaptive circuits such as neural networks represent a challenging approach which intends to take advantage of the rich functionality of nano-size building blocks and at the same time to manage variability.
In this context, functionalized carbon nanotube field effect transistors are of special relevance as they combine exceptional electrical performances with additional functionalities such as sensing and memory capabilities. In particular, coating such transistors with a thin film of photoconductive polymer adds decisive improvements in terms of optoelectronic properties: upon light excitation, we showed that these devices present large changes in conductance associated with a well controlled and non-volatile memory effect [1]. We established the critical role of charge trapping at the polymer-dielectric interface [2] in these memory-FETs.

In the present study, we show that Optically Gated Carbon Nanotube Field Effect Transistors (OG-CNTFETs) have all the required characteristics of a synapse, the basic building block for adaptive circuits. It requires demonstrating operation as 2-terminal devices with a memory effect, programmability, large dynamics and tolerance to variability. The capability to program multiple devices is also established and a way to implement these nano-synapses in large circuits is proposed.

Multiple OG-CNTFETs based on carbon nanotube networks and sharing the same output electrode were fabricated (Fig. 1). The use of nanotube networks allows the fabrication of reliable circuits with reasonable dispersion of their transfer characteristics The conductivity of each device can be tuned over several orders of magnitude using both light and electrical pulses on the input electrode [3]. Using a global illumination step followed by electrical stimuli at the input electrodes, the conductance of multiple devices can be very precisely programmed to arbitrary values as shown in figure 2. No-cross-talk between neighboring devices was observed at the considered scale.

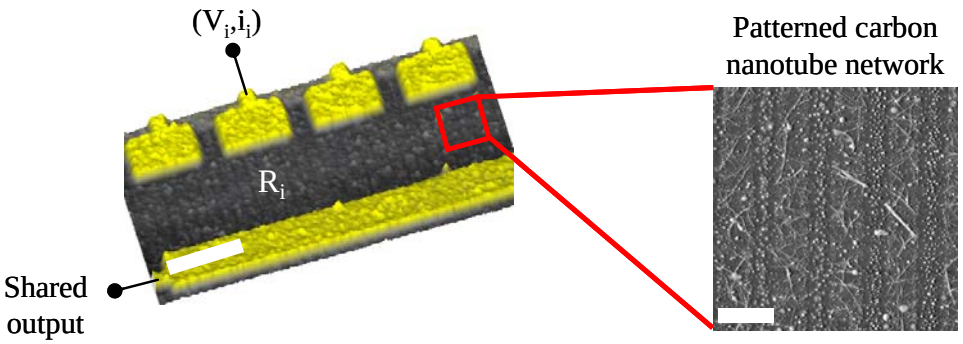

Figure 1: 3D view AFM image of a 4 OG-CNTFETs sharing the same output electrode. AFM image showing the CNT network used as transistor canal. Scales bars are respectively 4 µm and 800 nm.

We thus demonstrated that OG-CNTFETs act as 2-terminal like programmable resistor the resistivity of which can be adjusted within 3 orders of magnitude and then maintained in a non volatile way. Such programming scheme allows coping with the crucial issue of variability among as-built devices. Using experiments with aggressively scaled devices, we recently established that this programming step can be performed within the µs time range, thus allowing high speed writing. Detailed characterization of these scaled devices also brings new information on the charges trapping/detrapping mechanism and dynamics.

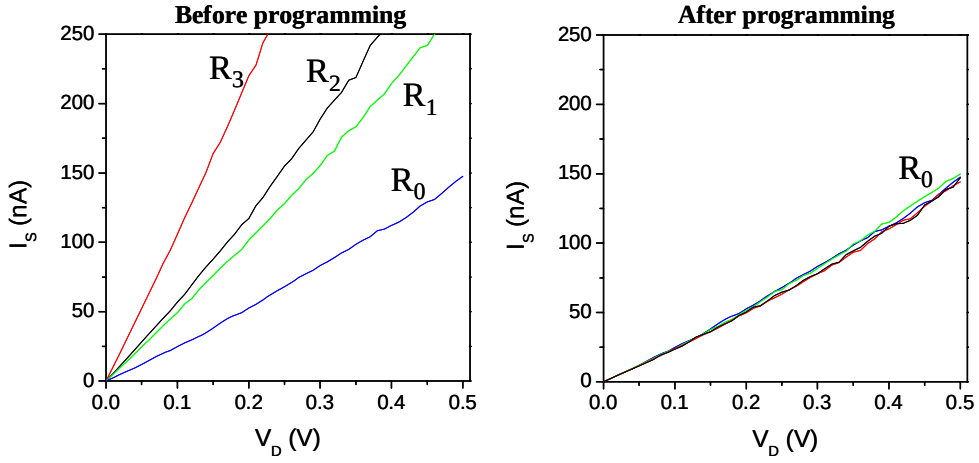

Figure 2: $I_S(V_{DS})$ characteristic of multiple OG-CNTFETs sharing the same output electrode. After the illumination step, each device has different conductance value. Using input electrode programming pulses, each device conductance is set to the same value.

As the process is compatible with integration above a CMOS layer, this strategy could allow implementing simple neural network-like architectures in which the nanotubes would play the role of synapses and the neurons would be implemented within the CMOS layer [4]. We will propose an original architecture based on OG-CNTFET synapses compatible with a massively parallel learning procedure.

References:

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