Poster

TECHNOLOGICAL DEVELOPMENT FOR STEP AND REPEAT IMPRINT LITHOGRAPHY

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The possibility of replication of the nanostructures of a hard stamp into a polymer was first proposed by S. Chou et. al. in 1995 [1]. Since then, nanoimprint lithography (NIL) has evolved from being a promising alternative method for nanofabrication [2, 3], to be, nowadays, a mature technique that allows obtaining nanometer scale features at wafer scale, with high reproducibility and throughput [4]. The applications taking advantage of NIL fabricated structures covers from micro/nano electronics, material sciences, or biology, just to cite some examples. In this communication, we will show several technological developments for the fabrication of interdigitated nano-electrodes using different imprinting-based aproaches.

Two different NIL methods have been developed. **Thermal NIL** process consists on embossing a deformable polymer above its glass transition temperature (Tg) with a hard stamp, cooling-down the system and releasing the pressure when the polymer is solid again. In **UV-NIL,** a transparent stamp is approached to the substrate, which is coated with a liquid photocurable pre-polymer or a very low molecular weight resist, so just a soft pressure is needed to fill the cavities with the liquid, that then is cured with UV light, so after releasing the stamp, the features are replicated in the polymer. On the other hand, the imprinting processes can be performed in a single imprint step of the whole sample (parallel printing) or by **step and repeat**, using smaller stamps and doing multiple replications in the wafer.

We are developing processes for thermal and UV step and repeat imprint lithography using an NPS 300 system from SET [5], recently installed at the IMB-CNM clean room. It is able to perform alignment with an accuracy of few hundreds of nanometers, which is important not only to carry out multiple step and imprint processes, but also to make structures in different layers. Several imprinting parameters are being optimized, such as the temperature of the stamp and chuck during imprinting. In the case of UV-NIL, the resist is dispensed locally for each imprinting step, so that it is cured at each local site. The imprinting process parameters needs to be studied and optimized according to the stamp geometry, structures depth and filling factor.

Several technological processes for **stamp fabrication** are also being developed. Figure 2 shows a silicon stamp fabricated by electron-beam lithography and reactive ion etching. Figure 3 shows an image of a transparent stamp, made in a novel polymer [7], for UV-NIL. More examples will be presented at the conference.

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References:

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[7] ORMOSTAMP from micro resist technology GmbH, Berlín. www.microresist.com

Figures:

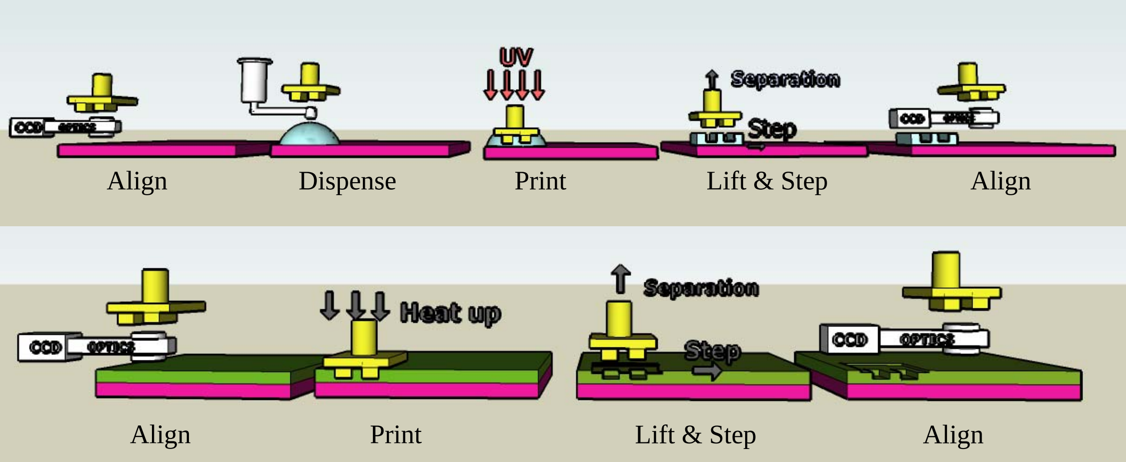

Figure 1. Scheme of UV-NIL process: align stamp and substrate, dispense the resist, print and UV cure, lift&step and align for a new imprint. Scheme of Hot Embossing process: align stamp and substrate, print applying pressure and heating up above the T_g of the polymer, lift&step and align for a new imprint.

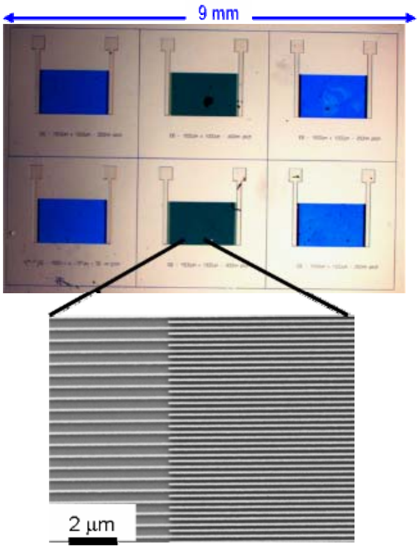

Figure 2. Silicon stamp containing six individual chips with structures of nanometric interdigitated electrodes. The stamp was fabricated by electron beam lithography, metal, lift-off, and reactive ion etching. The effective area of the digits is 1 mm x 1.5 mm. The pitch is varied from 250 nm to 400 nm, the electrode width is fixed at 150 nm, and the depth is 180 nm, as evaluated from AFM measurements.

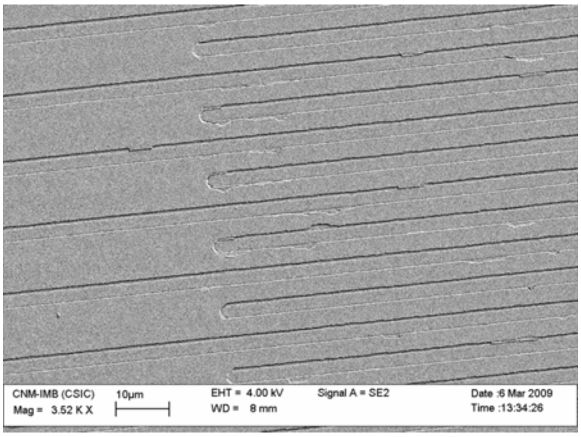

Figure 3. SEM image of the detail of one polymer stamp made of ORMOCOMP by replication from a silicon stamp. Depth of the features is 150 nm. Good uniformity is observed at chip level. The surface is covered with a gold layer to allow the SEM imaging. Process details will be shown at the conference.