Functional Model of Nanoparticle-Organic Memory Transistor for Use as a Spiking Synapse

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Emerging nanocomponents are of great interest to provide adaptability, high density and robustness for the development of new bio-inspired circuits or systems. Although CMOS Neuromorphic circuit was one of the most intense researches to bring the adaptability and robustness in the circuit beyond the conventional Von Neumann architecture in early 1990', CMOS technology could not provide the huge capacity to be scalable to biological levels because a great number of transistors are required to emulate the dynamical behaviors of biological synapse [1]. Nanoscale components are therefore of great interest to develop new neuromorphic circuits by replacing CMOS technology based synapse. The Nanoparticle–Organic Memory transistor (NOMFET) is one of the most promising candidates as it can exhibit dynamical behaviors similar to a biological synapse [2]. It could be very suitable to implement some natural synaptic learning mechanisms such as Spike-Time-Dependent-Plasticity (STDP) [3].

The NOMFET is composed of three terminals as the conventional MOSFET, Drain (D), Source (S) and Gate (G). The device is fabricated using a bottom-gate electrode configuration. Gold nanoparticles (NP) are immobilized on the surface of the inter-electrode gap before pentacene deposition. The conduction in the device is assured by holes, created in the thin film at the interface with the silicon oxide when a negative gate voltage is applied. In addition to rather classical transistor behavior, a negative gate voltage also positively charges the Au NPs. This has the effect of diminishing the channel conductivity of the device, because the charged NPs cause a repulsive electrostatic interaction between the holes trapped in the NPs and the ones created in the pentacene. The NOMFET therefore exhibits a short term memory and the charge retention time in the NPs can be as high as several thousand seconds [4].

A functional model is very useful for the design of hybrid Nano/CMOS circuit and architecture as it provides the interface between the fundamental physics and the electrical behaviors. We established the functional model of NOMFET for a two-terminal device configuration, as shown Fig. 1. The gate and the drain electrodes are driven by the same input voltage, a pulse train of a variable frequency. In this configuration, the dynamical behaviors of the NOMFET is a lot as a biological synapse: there is a competition between the charges provided to the NPs by the gate voltage pulses (resulting in a decrease of the drain-to-source current) and the natural NPs charge relaxation (which increases the current intensity until the NPs are fully discharged). When a new input pulse sequence occurs, the NOMFET exhibits either a depressing or a facilitating behavior, depending both on the duration between the pulses and on the charge level of the NPs. The current in the device is thus dependent on the history of the input signal; the maximum variation on our devices is close to 25% with 30V pulses amplitude.

Our model is iterative: the drain-to-source current response to a voltage pulse is calculated using essentially the width of the pulse, the current level at the previous pulse and the duration elapsed since then. Multiple measurements of the current response for voltage pulse sequences, including sequences with a variable frequency, are used to fit the model with experimental data,

to improve simulations accuracy. This iterative model has proved to be fully functional to simulate the dynamic behavior of NOMFET as a synaptic device (see Fig. 2). It is implemented in the Verilog-A analog hardware description language, which can be incorporated into the Spectre circuit simulator from Cadence to simulate mixed Verilog-A component and SPICE-level device circuits. This implementation also allows the model to easily integrate new experimental results.

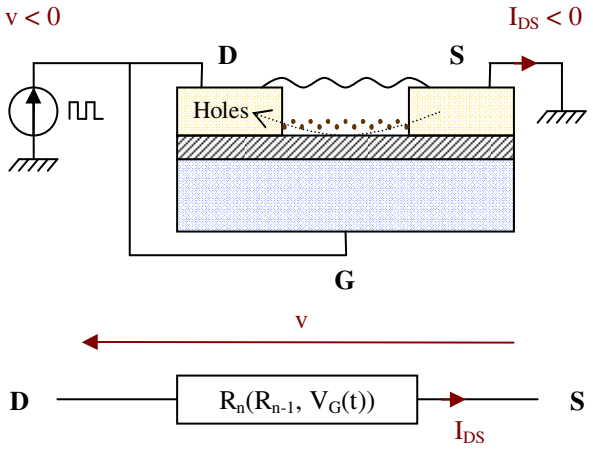

Figure 1: Device configuration used to establish our model and its electrical equivalent circuit (in linear regime). Input voltage v is a sequence of pulses of amplitude 30V. R_n is the equivalent drain-to-source resistance at the n-th pulse. R_n is dependent on the bias of the device and on the charge level of the NPs, reflected by the value of R_{n-1}.

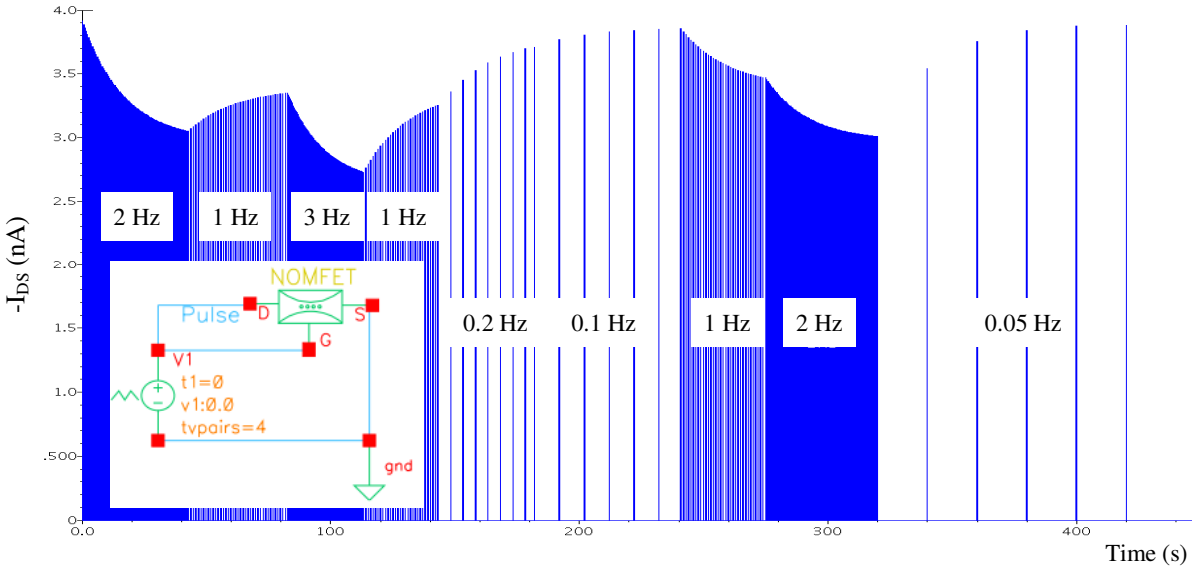

Figure 2: Transient simulation of spice NOMFET model with different input pulse train sequences (0.05 Hz – 3 Hz). Depending on the frequency and the historical weight or current level, depressing and facilitating behaviors can be simulated. NOMFET symbol and its test bench in the schematic editor of Cadence are shown as well.

Hybrid NOMFET/CMOS neuromorphic architectures are under investigation in our laboratory and future work will include model refinement, synapse-to-neuron interfacing and neuronal architecture simulation.

References:

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