Improvement of TFT properties by hydrogen defect passivation for high performance flexible electronics device application

Musarrat Hasan[1], Houk Jang[2], Sang-Hee Ko Park[1], Joon-Myong Lee[3]. Min-seok Jo[3], Jae-Bon Koo[1], Kyong-Ae Lee[2], Hyunsang Hwang[3], Jong-Hyun Ahn[2], Yong Hae Kim[1], *Seung Youl Kang[1]*

[1]Electronics and Telecommunication Research Institute, Convergance Components & Materials Research Laboratory, Daejeon; [2]Sung Kyun Kwan University, Suwon 440-746;

[3] Gwangju Institute of Science and Technology, Gwangju 500-712; Republic of Korea.

musarrat@etri.re.kr

Introduction: Electronic devices on flexible organic substrate have a huge market in the near future in the form of flexible display, RF ID tags, solar cells and various bio-systems.[1] But due to the limitation imposed by sustainable temperature it is a challenge to grow quality dielectric for transistor application for high mobility device. The dielectrics grown at low temperature (<200^{o}C) contains lots of defect sites. To improve the device properties, successful defect passivation is absolute necessity. Hydrogen (H_2) has been known for years to passivate the defect sites far more effectively, especially near the interface region.[2,3] In this work we have investigated impact of H_2 annealing on the device performance of single-crystal Silicon active layer device on flexible substrate.

Experimental: The fabrication steps started with the doping process of phosphorous spin-on dopant at 950^{o}C on SOI wafer. The underneath SiO_2 layer was etched out by HF solution (49%) and Si ribbons were detached. After that the Si layer of 290 nm was transferred to the polyimide (PI) plastic substrate via PDMS stamping process described in many other recent publications.[4] After the transfer process, Alumina (Al_2O_3=110nm) was deposited in an ALD system at 150^{o}C. Chromium (Cr) and gold (Au), 5 nm and 100 nm respectively, were deposited to complete the TFT fabrication process (fig. 1). To improve the contact between the metal and S-D, a forming gas annealing process (FGA; H_2=3 wt%, rest N_2) was performed at 200^{o}C and 1 atm pressure. To improve the oxide interface quality subsequent high pressure pure hydrogen annealing (HPHA) was performed for the same sample at 20 atm pressure where pure H_2 was used.

Results and discussions: Fig. 2 shows the transfer characteristics of the as deposited Al_2O_3 device at V_d of 0.1 volt. The threshold voltage (V_{th}) was calculated from the x-axis intersection of the square root of the transfer curve. Fig. 3 shows the I_d-V_g result at different gate voltage, but the output current is mere few microamperes. The sample was then annealed at 200^{o}C in 1 atm pressure in FGA containing 3% H_2 and 97% N_2. The current increased over 100 times, giving an on/off ratio of >10^5 (fig. 4). The mobility improved to 140 cm^2/V.s. Hydrogen passivate the defects present at the metal-dieletric interface during metal deposition. This is known as the "Sintering" step in the silicon industry for long time.[5] The oxide defects present at the Si/oxide interface and also the bulk defects are also important and can be effectively passivated by H_2.

To passivate the defects more aggressively, H_2 annealing was done at pressure as high as 20 atm (HPHA) at 200^{o}C of the same sample in pure H_2 atmosphere. A specially built chamber was used for this kind of experiment. Fig. 4 compared the HPHA data with that of as deposited and FGA data. Compared to the FGA sample further improvement especially in the off current has been observed. This indicates better passivation of the oxide defects by more injection of H_2 at a very aggressive manner. Fig. 5 shows transconductance curve (g_m) of devices after each step. Significant improvement of g_m is achieved after FGA and consequent HPHA step. Fig. 6 shows the ouput characteristics after FGA and subsequent HPHA treatment. All the properties are summarized and compared in table 1. The on/off ratio, g_m, mobility, subthreshold slope, all shows tremendous improvements after annealing in hydrogen atmosphere. These results are encouraging for low-temperature plastic TFT technology for flexible device application with mobility close to 200 cm^2/V.s.

Next the interface charge density has been measured using the charge pumping (CP) method. Along with CP, the V_{th} shift was also monitored under constant voltage stress. The applied voltage stress was +10 V. The voltage sweep was performed from -10 V to +10 V with V_d 0.1 V. For the CP method a voltage pulse was applied from base voltage of -7 V to top voltage of -4.5 V. The falling and rising time was fixed to 100 ns. The pulse width was 1 μs. The stress was applied for 1000 s and both I_d-V_g and CP current was measured at different interval. With applied stress, the V_{th} shift in the positive direction and the total shift after certain stress time are depicted in Fig. 7 against time. Fig. 8 shows the interface charge density (N_{it}) after each stress cycle. A low N_{it} values in the range of $2x10^{11}$ cm^{-2} has been found. The N_{it} after each stress also does not change, which indicates the voltage shifts that is observed is not related to the interface charge traps. The hydrogen annealing effectively passivated the interface traps and the mobility improvement primarily is due to the interface charge passivation. The V_{th} shift may be mainly due to the traps in the bulk oxide region.

Conclusion: High mobility single crystal Silicon TFT with medium-k dielectric has been fabricated. The device performance was improved after H_2 passivation annealing. The maximum process temperature was 200^{o}C suitable for flexible device applications. The understanding and improvement of higher-k device gate insulator by post metal annealing for flexible device technology performed in this study is promising for future.

References:

[] R. H. Reuss, et. al.; Proceedings of the IEEE, v. 93, p. 1239 (2005)

[2] A. Kamgar, et.al.; IEEE Elec. Dev. Let. Vol. 24, p. 448 (2003)

[3] P.J. Chen, et. al.; Jour. Appl. Phys. Vol. 86, p. 2237 (1999)

[4] D.-H. Kim, et. al.; IEEE Elec. Dev. Lett., Vol. 29, p. 73 (2008)

[5] K. Onishi, et. al.; IEEE Trans. Elec. Dev., Vol. 50, p. 384 (2003)

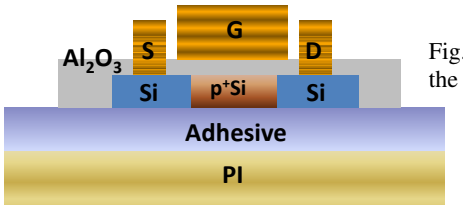

Fig. 1: Schematic of the device structure

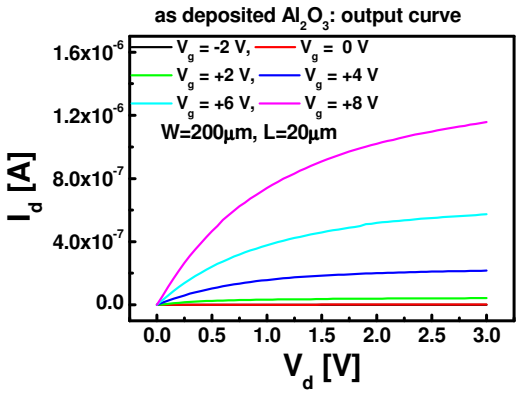

Fig. 3: I_d-V_d characteristics of the as-deposited Al_2O_3 device

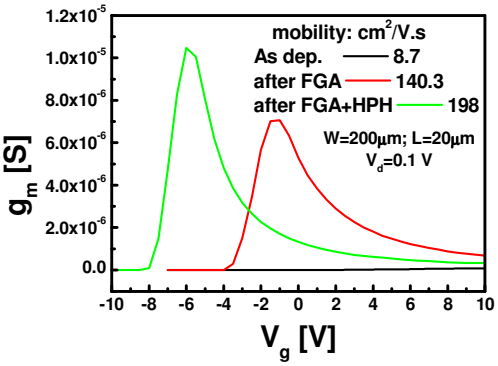

Fig. 5: Comparison of the g_m characteristics of the device data shown in fig. 4.

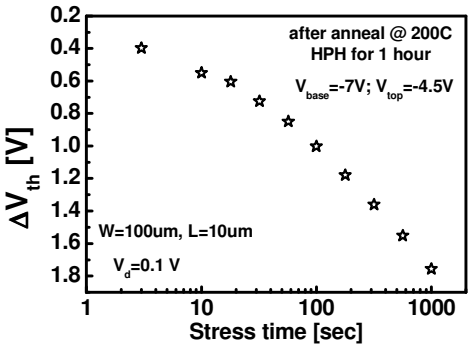

Fig. 7: Total V_{th} shift after HPHA measured at different time interval

Table 1	As dep.	FGA	HPHA
On/Off ratio	$>10^3$	$>10^5$	$>10^6$
Gm_{max} (S)	$8.2X10^{-8}$	$7.05X10^{-6}$	$1.2X10^{-5}$
Mobility (cm^2/V.s)	8.7	140	198
SS (V/dec)	3.22	0.36	0.28
V_{th} (Volt)	0.2	−3	−7.3
Hysteresis (Volts)	8	7.5	3.1

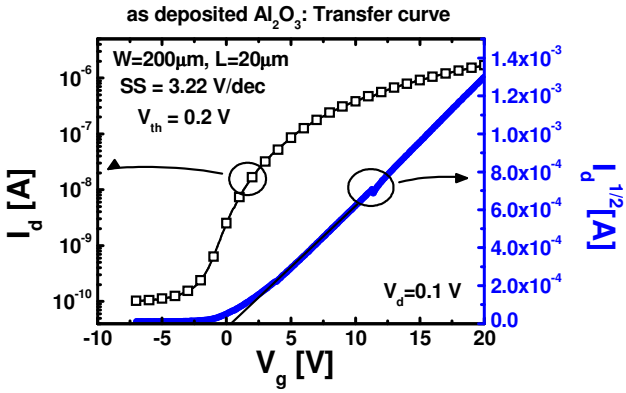

Fig. 2: I_d-V_g characteristics of the as-deposited Al_2O_3 device

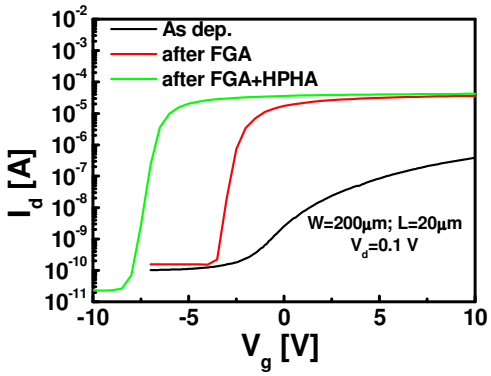

Fig. 4: Comparison of the I_d-V_d characteristics of the as-deposited and after different annealing steps.

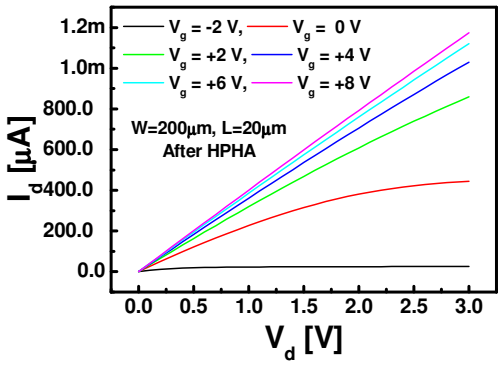

Fig. 6: Output curve after HPHA at 200°C

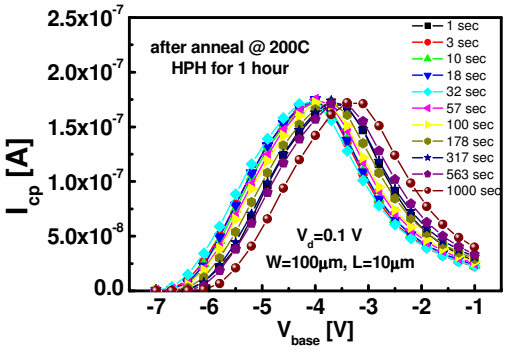

Fig. 8: Interface trap density measured in CP method does not change with stress implying V_{th} shift is not due to interface traps.