

EXPLOITING THE NEGATIVE CAPACITANCE REGION OF FERROELECTRIC OXIDES FOR SURFACE POTENTIAL AMPLIFICATION IN METAL-FERROELECTRIC-INSULATOR-SEMICONDUCTOR DEVICES

David Jiménez^{1}, Enrique Miranda¹, Francesca Campabadal², Joan Marc Rafi², and Florencio Sánchez³*

¹*Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona*

²*Instituto de Microelectrónica de Barcelona (IMB-CNM-CSIC)*

³*Instituto de Ciencia de Materiales de Barcelona (ICMAB-CSIC)*

(*) david.jimenez@uab.es

One of the most severe problems pointed out by the microelectronics industry in the *International Technology Roadmap for Semiconductors* is the increasing power dissipation at the chip level due to the relentless scaling down of the transistors dimensions [1]. This problem has been referred to as the **power crisis** in the microelectronics industry and the main reason behind can be traced back to the difficulty of reducing the transistor inverse subthreshold slope (S), which shows an *apparent* limit (because of thermodynamics constraints) of 60 mV/decade. Nevertheless, theoretical studies show the feasibility of achieving **S<60 mV/decade** by replacing the gate insulator dielectric with a **ferroelectric material** [2]. This kind of materials exhibits a **negative capacitance** region that, according to theoretical considerations, could result in surface potential amplification. This approach presents two important advantages: the transistor operation principle is retained as well as the potential compatibility with CMOS (Complementary Metal-Oxide-Semiconductor) fabrication technology.

From a practical viewpoint, integration of a ferroelectric oxide film directly on silicon is extremely difficult because of the mismatch between lattice parameters, interdiffusion, and chemical reactions that degrade the properties of the oxide, the underlying silicon, or both, yielding electrically active defects at the semiconductor interface [3]. To our knowledge, only a very recent publication has reported the growth of a good quality ferroelectric layer of SrTiO₃ on silicon [4]. To overcome the integration problem, the usual approach consists in using a thin insulating buffer layer that almost perfectly matches the silicon substrate with the ferroelectric oxide film [5]. Considering the state of the art on ferroelectric oxide integration, we have focused our research on a Metal-Ferroelectric-Insulator-Semiconductor (MFIS) gate stack. In this work, we have theoretically investigated the referred system, and explored the optimal geometrical parameters needed for the experimental observation of the surface potential amplification effect (Figure 1).

References:

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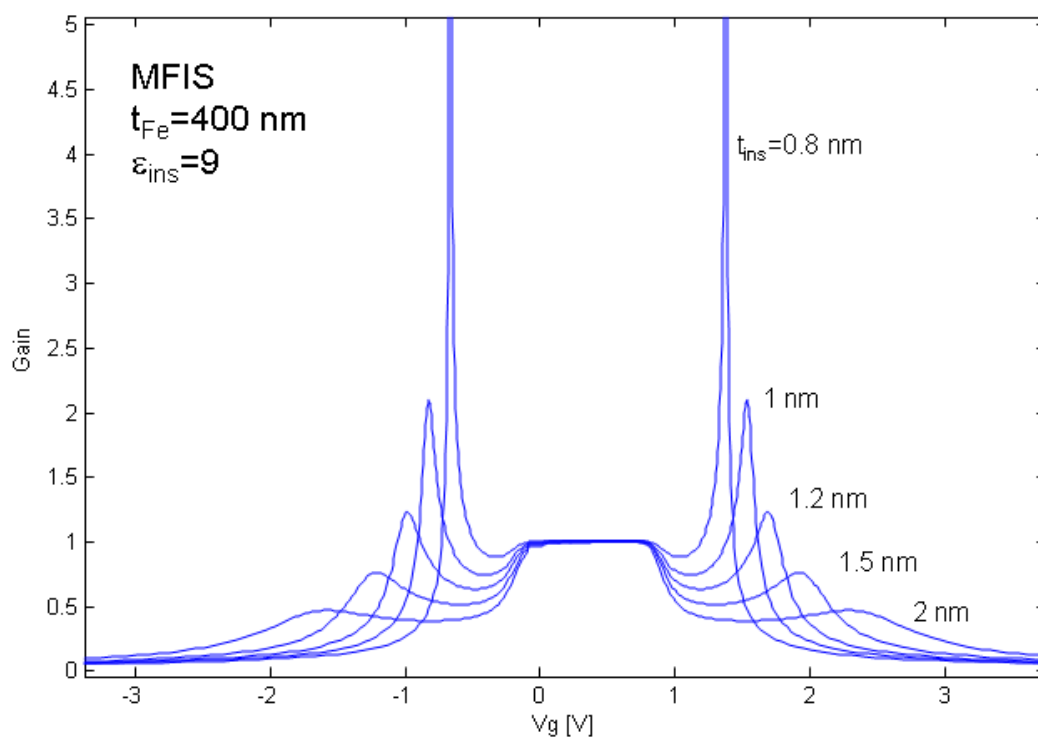


Figure 1. Predicted gain of a MFIS gate stack, looking for surface potential amplification. A large gain (~ 5) should be possible with an insulator buffer layer 0.8 nm-thick and dielectric permittivity of 9. As shown in this figure, degradation of the gain is severe as the insulator thickness increases. Above 1.2 nm the gain turns out to be smaller than unity for any applied gate voltage. At this critical value the surface potential amplification would not be observable