Poster

CONDUCTIVE AFM ANALYSIS OF THE TRAPPING PROPERTIES OF SIO_2 TUNNEL LAYERS FOR NON-VOLATILE MEMORY DEVICES

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Abstract

In this work, the impact of an electrical stress on MOS structures with a 9.8nm thick SiO_2 layer has been investigated at device level and at the nanoscale with Conductive Atomic Force Microscopy (CAFM). The goal is to correlate both kinds of measurements when studying the degradation of tunnel oxides of non-volatile memory devices. In particular, the generation of defects and its impact on leakage current and charge trapping have been analyzed through spectroscopic measurements and current images.

Keywords: Conductive Atomic Force Microscopy, electrical characterization, non-volatile memory devices.

1. Introduction

To continue with the scaling down of the dimensions of memory devices, their electrical properties and reliability have to be further investigated. In particular, the degradation of the tunnel oxide due to the programming operations (which leads to a reduction of the device reliability) must be studied in detail. However, standard characterization techniques only give averaged information of the electrical properties of the devices. To obtain more detailed information, new techniques with higher spatial resolution must be considered. In this work, a CAFM (Conductive Atomic Force Microscope) [1,2] has been used to investigate, at the nanoscale, the electrical properties of SiO_2 tunnel oxides that have been previously subjected to an electrical stress using standard characterization techniques at wafer level.

2. Experimental

The samples are MOS capacitors (2.5µm x 2.5µm sized) with a 9.8nm thick SiO_2 dielectric and poly-silicon gate. These capacitors have been stressed by applying constant current stresses (CCS). In particular, CCS of $J=10^{-2}$ A/cm² and $J=10^{-1}$ A/cm² during 100 seconds have been applied to different structures. Some of the capacitors, without being stressed, will be considered as reference. In the V-t curves measured during the stress, an increase of the applied voltage has been observed, which suggests trapping of negative charge in the oxide. In the harder stress, some structures experienced breakdown (BD), registering a sudden drop in the V-t curve. After the stress, the polysilicon layer has been removed with a very selective etching to avoid any damage of the oxide. Afterwards, the AFM tip was located on the gate area and CAFM measurements have been performed. When the tip scans the surface, simultaneously to the topography, current maps are obtained by applying a constant voltage between the tip and the sample and I-V curves can be measured on particular oxide locations (area of ~$300nm^2$).

3. Results

We will start investigating the nanoscale electrical conduction of the different samples from spectroscopic measurements. I-V characteristics were measured at different positions with the tip of the AFM. Low voltages have been applied during these monitors in order to modify the less as possible the previously induced degradation. Figure 1 shows the statistical distribution of the onset voltage (voltage needed to measure a current of 10pA) for the different structures after measuring I-V curves on several positions. Note that the mean value of the onset voltage does not show significant differences between the samples, although it is slightly larger for those previously stressed. Since the larger the onset voltage, the lower the conductivity, this slight increase of the onset voltage could be attributed to the charge trapped in the oxide during the pre-stress (as already observed in the V-t measurements at device level). On the other hand, the rms value of the onset voltage increases with the stress, which suggests that the electrical conduction is less homogeneous in stressed structures than in fresh oxides. This behavior can be related to the generation of defects during the pre-stress. In those positions with a larger concentration of defects, the conduction could be increased due to trap assisted tunneling (TAT) or decreased due to charge trapping after stress, leading to a larger dispersion of the onset voltage and therefore, to a larger rms value. Note that, although the global electrical conduction decreases (as observed in the poly-gated devices during the stress), the inhomogeneity of electrical conductivity

increases. It is important to emphasize that this inhomogeneity can not be detected from standard techniques: only AFM techniques allow these observations due to its nanoscale spatial resolution.

To perform a more detailed analysis, the electrical conduction has been further studied from current images obtained with the CAFM. To investigate the electrical homogeneity, images were obtained by applying the gate voltage necessary to measure current just above the noise level (that is, by applying the same electrical field). Figure 2 shows current images obtained by scanning the surfaces of, (a) a reference oxide and (b) and (c) oxides stressed at $J=10^{-2}$ A/cm² and $J=10^{-1}$ A/cm², respectively. The voltages needed were 10.2 V for figures 2a and b, and 10.7 V for figure 2c. In (c) no BD spots where observed (in case they were triggered) since the scanned area is much smaller than the capacitor size and BD is a local phenomenon. Due to charge trapping, after the stress, higher voltages are necessary to measure the same current for the samples subjected to the larger CCS stress. However, this is not the case of the sample stressed at $J=10^{-2}$ A/cm^2; this effect could be attributed to the fact that there can be other experimental factors (changes on the tip conductivity, contact area, small local variations of the oxide thickness…) that can have a larger impact on the electrical conduction. The statistical analysis of these images allows to compare the homogeneity of each sample. Note that the rms value of the current is larger on stressed samples (as already observed from the I-V curves). In these samples, some leaky sites appear which show larger currents than the rest of the oxide (darker areas in the images). A statistical analysis of the leaky sites with a current 1pA above the background has been done (fig.2 table). Note that the number, the mean current and the mean area of the leaky sites after the stress are larger than in the fresh structure. This result suggests that, although there is a certain amount of trapped charge in the oxide after the stress, which leads to smaller average currents when applying the same gate voltage, at some sites, the stress also leads to an increase of current related to TAT through the generated defects.

4. Conclusion

The electrical properties of SiO_2 tunnel oxides of non-volatile memory devices subjected to different device level stresses have been studied at nanometer scale using a CAFM after poly-silicon gate removal. I-V curves have been measured with the CAFM at different oxide locations. In the stressed samples, smaller conductivities but larger inhomogeneities are observed. These results are further supported by the current maps measured at the nanoscale with the CAFM. Additionally, the current images show that although after the stress the mean current decreases, some leaky sites appear. Therefore, most of the defects generated during the stress act as trapping sites (which lead to the increase of voltage during the CCS), but some of them locally increase the conductivity of the sample leading to Stress Induced Leakage Current (SILC). At device level, however, SILC is masked by the decrease of the conductivity due to trapping, since standard tests are only able to measure average properties of the layer.

References

[1] A. Paskaleva, V. Yanev, M. Rommel, et al. , J. of App Phys, Vol. 104(2) 024108 (2008).
[2] M Porti, M Avidano, M Nafria, et al., J. App Phys 101(6) 064509 (2007).

Figures and figure captions

Level of stress	Mean (V)	Rms (V)
Reference	10.47	0.13
10^{-2} A/cm^2	10.69	0.26
10^{-1} A/cm^2	10.65	0.25

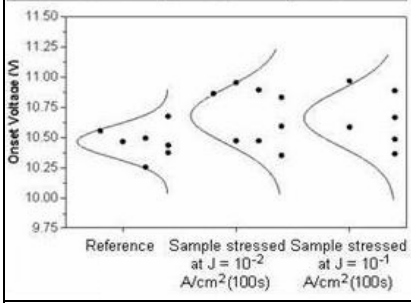

Fig.1. Statistical analysis of the onset voltage.

Sample	Current roughness (pA)	# Sites	Mean current (pA)	Mean area (nm^2)
(a)	0.26	90	2.0	44
(b)	0.55	104	2.3	150
(c)	0.57	108	2.1	81

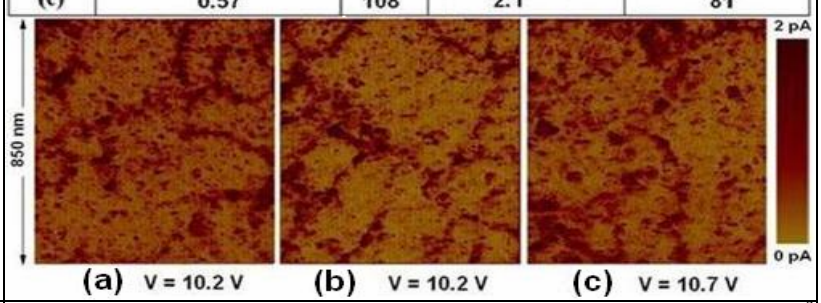

Fig.2. Current images obtained on fresh capacitors (a), oxides stressed at $J=10^{-2}$ A/cm² (b), and $J=10^{-1}$ A/cm² (c). Table: leaky sites with a current larger than 1pA.