Inconsistent behavior of electrical conductivity in Pd thin film as a function of film thickness

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The electrical conductivity of thin metal films has become a problem of increasing importance because of their widespread use in electronic devices. Generally, the resistivity of thin films is described in terms of scattering of the conduction electrons at the external surfaces. The theoretical basis for this phenomenon was given by Thomson [1]. The standard theory for calculation the electrical conductivity of thin films is commonly described by Fuchs [2] whose work was later extended and corrected by Sondheimer [3]. More attention into the microstrucrure of thin films has led to appreciation of the fact that not only the external surfaces, but also the grain boundaries will modify the resistivity [4]. The aim of the work is to investigate the effect of thickness variation in Pd thin films on interfacial properties, surface topography and electrical conductivity.

Pd was evaporated on top of the SrTiO3 (STO) by means of electron beam physical vapor deposition (EBPVD). Different thicknesses of Pd were obtained with increasing distance between evaporation source and substrates. Deposition was conducted with 1.6 KV potential, 200 mA emission intensity, and the pressure better than 4×10^{-6} mbar. Substrate temperature was set at 300º C to increase the crystallinity of the film. The crystalline structure has been determined by X-Ray Diffraction (XRD) analysis in θ-2θ scan by means of a 4-circle X-ray diffractometer with Cu-Kα radiation. Atomic force microscopy (AFM) was utilized to clarify the growth mode of the Pd on top of the STO. Electrical conductivity was measured by means of two conductive tips and amperage - voltage plot (I-V) was attained. Besides, X-ray Photoelectron Spectroscopy (XPS) was used in depth analysis mode to elucidate the interfacial phenomena.

XRD results of Pd showed the growth of Pd on (111) crystallographic direction. Furthermore, it is reported that all metals with FCC structures such as Au and Pd, tend to have a natural preference in (111) orientation during the growth which is strongly due to the low number of the bonds with neighboring atoms in these low dense plans. Indeed, low lattice mismatch between Pd and STO could be the main reason for inconceivable adhesion properties [15]. Fig (1) dedicated to AFM topographic imaged for hillocks which appear in the different thickness of Pd thin film. As shown in Fig 1 (a), same height of hillock has been seen in 25 nm and 45 nm thin film of Pd while the hillock height decreased in 65 nm thickness. However, 100 nm Pd thin film showed the coarse and height hillocks. Indeed, the total area of the hillocks is minimum in 45 nm film in compare with the other thin films. This might roughly illustrate the lower surface roughness of 45 nm Pd film in compare with three other samples. In fact, the surface roughness introduce an extra degree of electron scattering called surface scattering which the decrease dramatically the electrical conductivity of the thin films. Therefore, the numerical amount has been used to measure the surface roughness of Pd thin film with 45nm thickness meanwhile Root-Mean-Square (RMS) roughness of the film was calculated around 4.6 nm roughness that could be subjected as a smooth film with respect to evaporation method. Fig 2 shows the electrical conductivity of different thicknesses of Palladium and consists of four selected thickness means 25nm, 45nm, 65nm, and 100nm. As shown in fig 2, it seems that Pd with 25nm thickness wasn't conductive due to partly growth of the film that happened because of low thickness. Basically, it is well-established that with increasing the thickness, resistance of the thin films will decrease. Thus, it was expected that electrical resistance of 45nm thickness film is more than 65nm thickness Pd film but it quashed, just in case. Indeed, Pd thin film with 100nm thickness was showed the lowest electrical resistance as was expected.

Fig 3 (a-c) showed the XPS signals of 45 nm thickness of Palladium thin film. As shown in Fig 3 (a), displays the corresponding Pd 3d features in as annealed sample. Appeared signal in 336.2 eV consists of Pd $3d_{3/2}$ which its intensity decreased with increasing sputtering time. Fig 3 (b) showed the Oxygen behavior in the interface of Pd and $SrTiO_3$. As shown in fig 3 (b), low concentration of Oxygen has been seen in the layer while raised with increasing the sputtering time which has been shown clearly in fig 3 (c). This phenomenon could be because of relaxation process due to breaking the bonds between oxygen and Sr, happened on the interface of Pd-STO. It seems, porosity of Pd magnified oxygen penetration and an unknown composition of Palladium oxide was appeared. Mainly, Palladium oxide acts as an insulator and increase the resistance of the films, dramatically. It would be a competition between the increasing the thickness and increasing the stress in the interface to govern the electrical resistance. It seems, existed stress governed to electrical conductivity in the thickness range between 30nm to 70nm.

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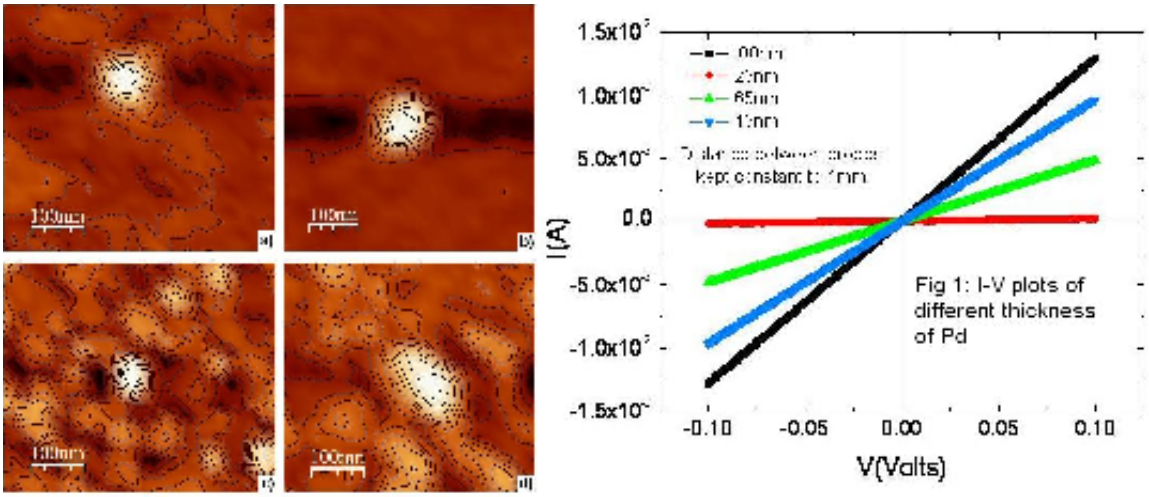

Fig 1: AFM 3D image of different thickness of Pd

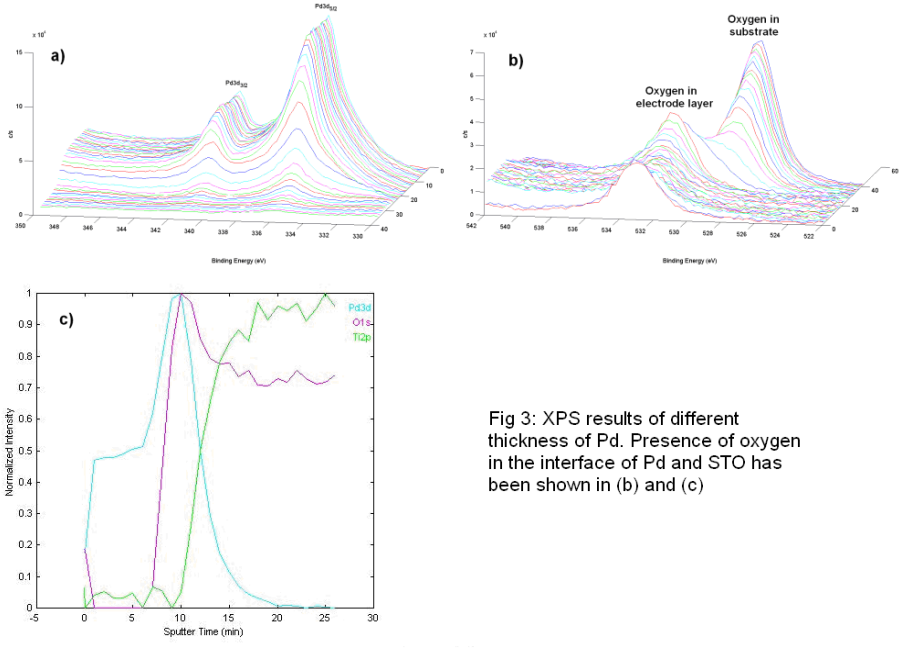

Fig 3: XPS results of different thickness of Pd. Presence of oxygen in the interface of Pd and STO has been shown in (b) and (c)