Non volatility and GHz magnetization dynamics in magneto-electronic devices, from memory to logic

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nanoICT coordination action

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UNIVERSITE PARIS-SUD XI

on work cited here:

Advanced Research Laboratory, Hitachi, Tokyo (Japan)

J. Hayakawa, K. Ito, H. Takahashi

tunnel junctions fabrication, micromagnetic modelling

Laboratory for Nanoelectronics and Spintronics, RIEC-Tohoku University , Sendai (Japan)

S. Ikeda, H. Ohno

magnetic tunnel junctions fabrication

Hitachi Almaden (USA)

J.A. Katine, M.J. Carey,

spin valve nanopillars fabrication

University of California, San Diego (USA)

E.E. Fullerton

spin valve films growth for DW studies

LPS Orsay

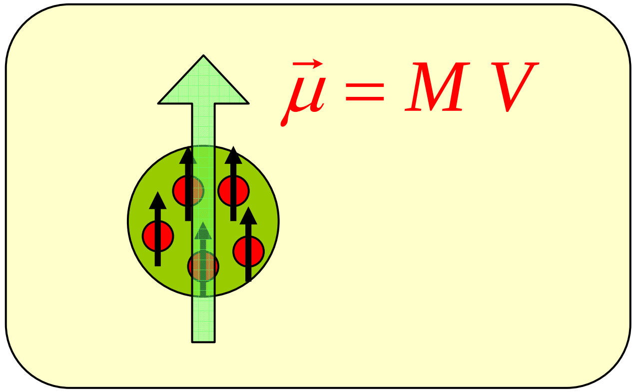
J. Miltat, J. Ferré

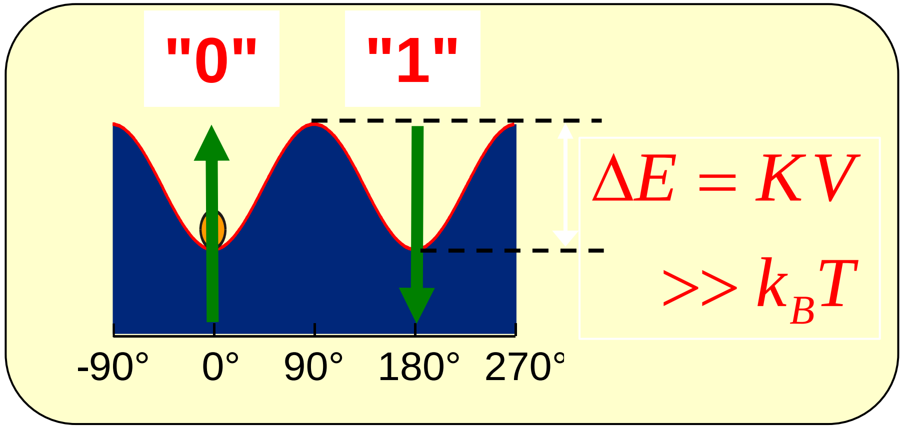
micromagnetic modelling, DW physics

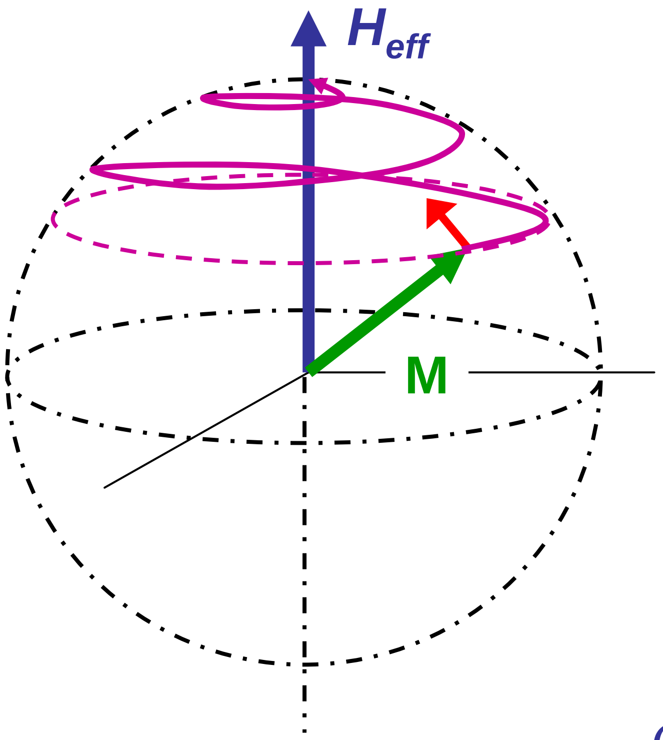
etc…

"localized" atomic magnetic moment picture

Exchange interaction	*Magnetic anisotropy energy*
tends to keep parallel the atomic moments	**total energy changes with the orientation of *M***
"magnetization" *M* in ferromagnets = *magnetic moment per unit volume*	**magnetic storage of the information**







Damped precession **of the magnetization M around its equilibrium axis**

- **precession frequency:** $f = f_0 H_{eff}$

f_0 = 28 MHz / mT (= 2.8 GHz / kOe)

- **magnetic energies ➔ effective field H_{eff}**

- **the Landau-Lifshitz-Gilbert (LLG) equation**

$$\frac{d\vec{M}}{dt} = -|\gamma|\mu_0 \left(\vec{M} \times \vec{H}_{eff}\right) + \frac{\alpha}{\|\vec{M}\|}\left(\vec{M} \times \frac{d\vec{M}}{dt}\right)$$

friction torque (damping)

The necessary compromise in magnetic recording

increase
recording density

reduce
bit volume V

reduce
writing power

thermal stability :

$\Delta E = KV >> k_B T$

increase K

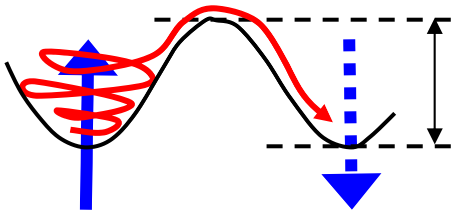
writing :

$H_{writing} \sim K$

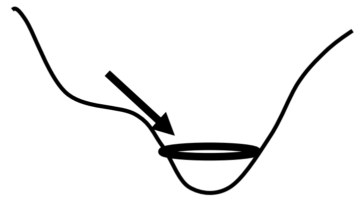
reduce K

X

Research



$\Delta E = K\,V$



intrinsic soft error (Néel-Brown)

ex: *10 years stability with error rate <10^{-6}*

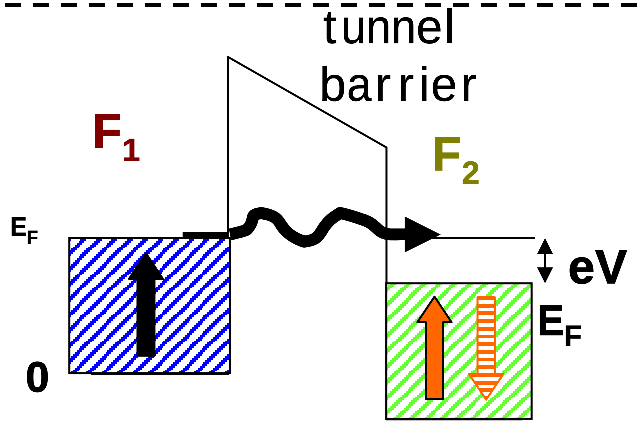
➔ $K\,V > 54\,k_B T$

switching can be fast

(precession ~a few GHz)

Reading: The magnetic tunnel junction

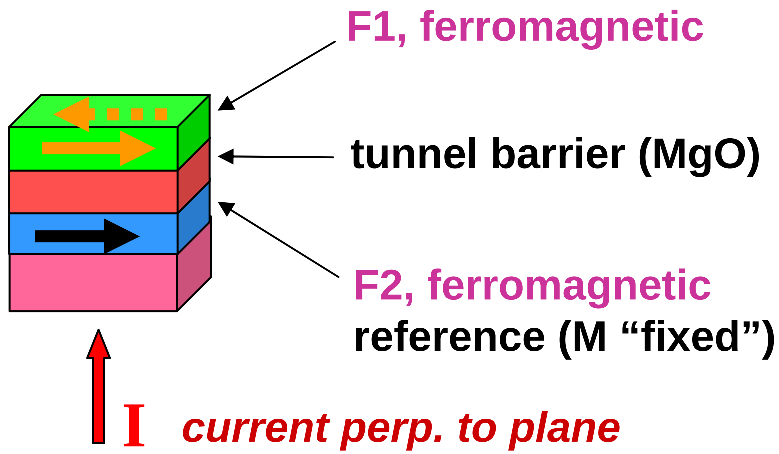
Jullières 1973 ; Moodera 1995



spin dependant tunneling:

$$R_{\uparrow\downarrow} \neq R_{\uparrow\uparrow}$$

magnetic tunnel junction



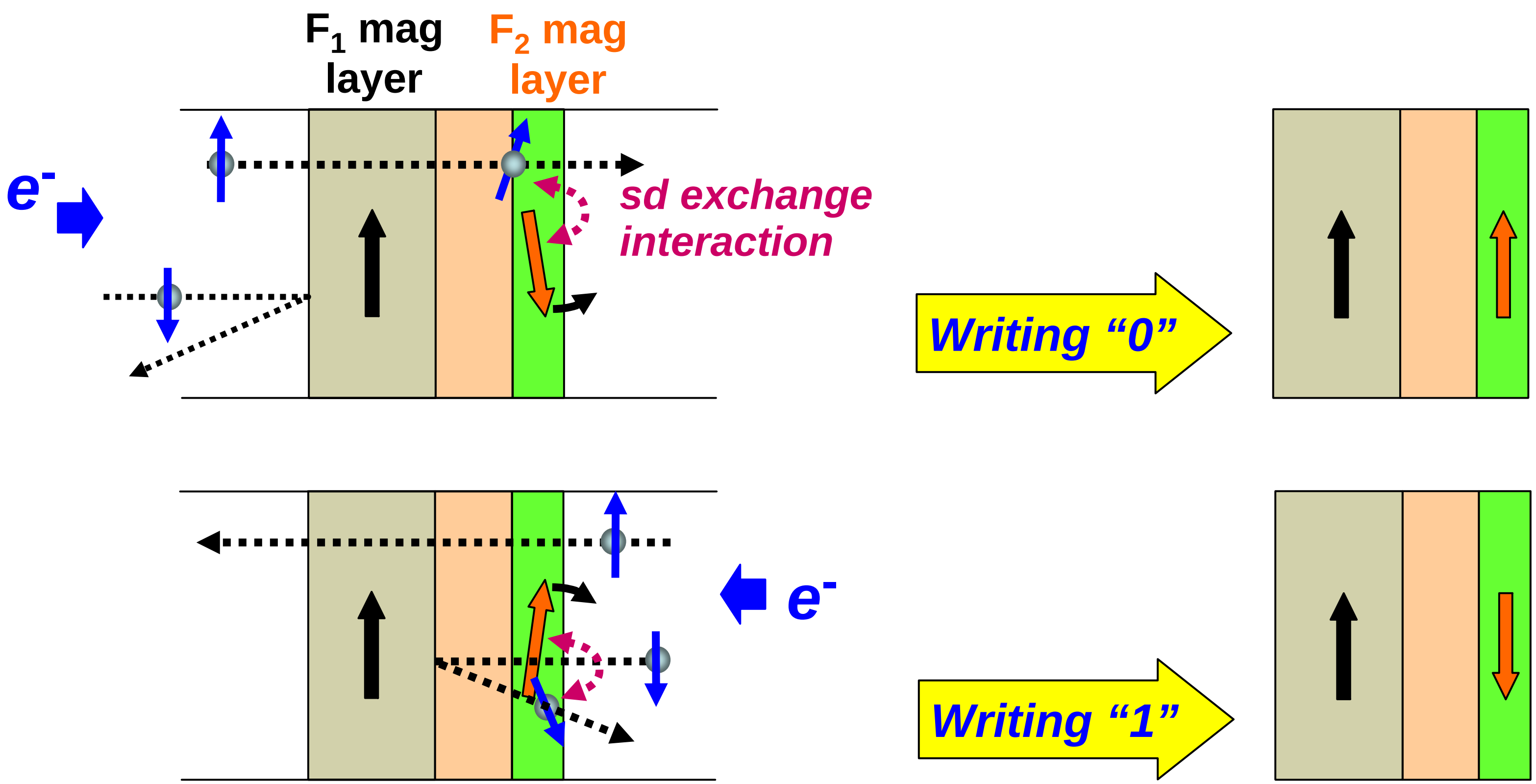
$\Delta R/R_{\uparrow\uparrow}$ ~ 600% (highest value @RT)
130 to 200% (practical)

a convenient device to integrate magnetic storage in CMOS electronics
➔ the magnetic RAM

Writing: Spin Transfer Torque switching

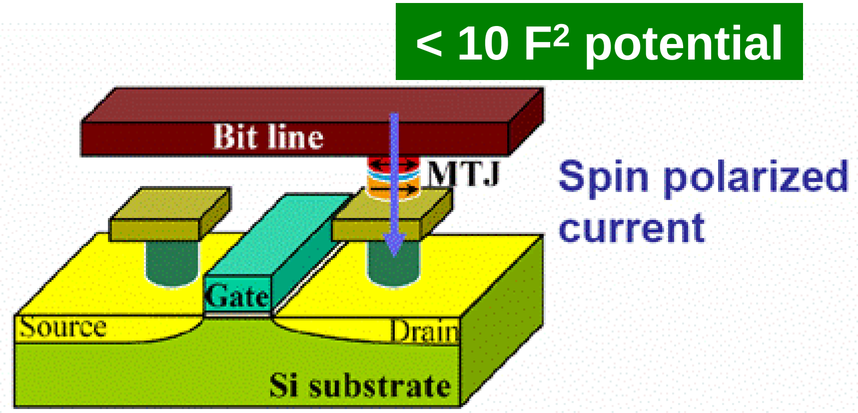
J. C. Slonczewski, JMMM 159, L1 (1996)

exchange interaction between the spin of conduction electrons and M



writing by a current density ➔ ~scalable

From conventional MRAM...
to "spin transfer" MRAM



<u>Demo chips of « Spin »-RAM:</u>
SONY, IEDM Dec. 2005
HITACHI, ISSCC March 2007)

➔ *simple " integrated " architecture, above CMOS technology,*

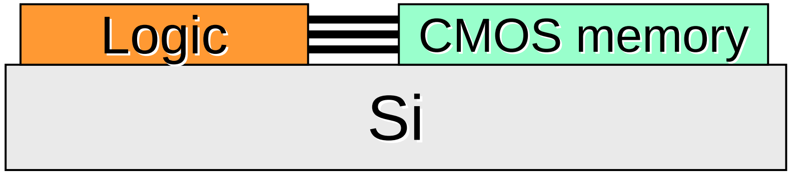
➔ *"write" driven by a current density, potential for :*

- *downscaling down to 20nm (Li et al., DATE'09 conf.)*
- *" moderately high " density (<10 F^2),*

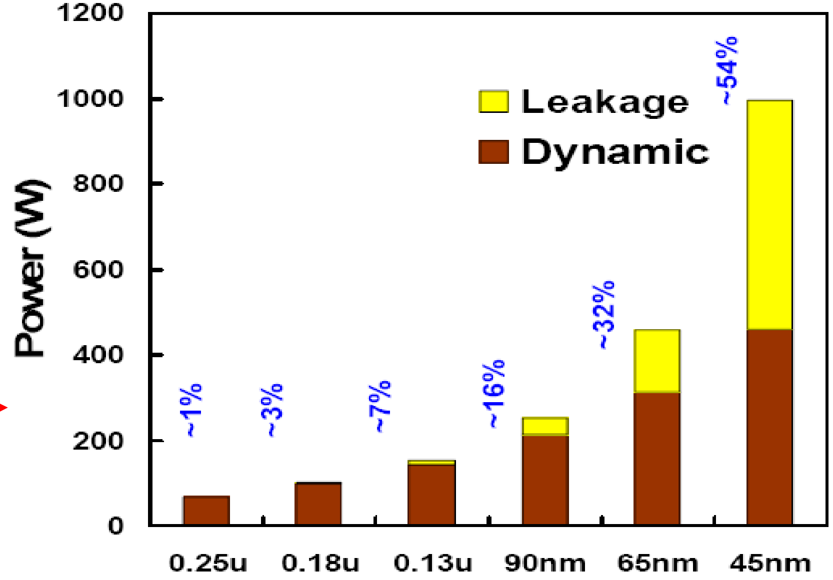
➔ *" fast " (10-100 ns)* : main advantage of M-RAM versus other NV-RAM

- but : more costly to fabricate (magnetic back end)
  and much less dense than Flash (soon 1.3 F^2 / bit !!!)
  or other new NV-RAM (PC-RAM, RRAM, ...)

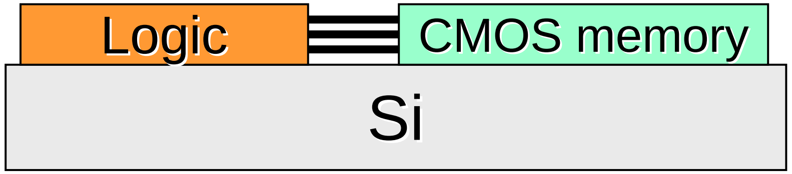
<u>With CMOS technology only</u>:

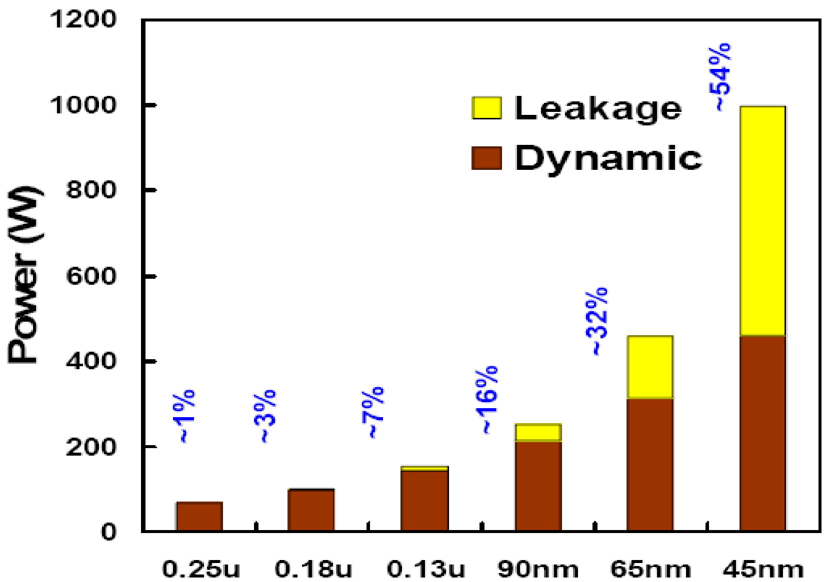


Slow communication between
logic and memory
-few long interconnections
-complexity of interconnecting paths
-larger occupancy on wafer
-large static dissipation →

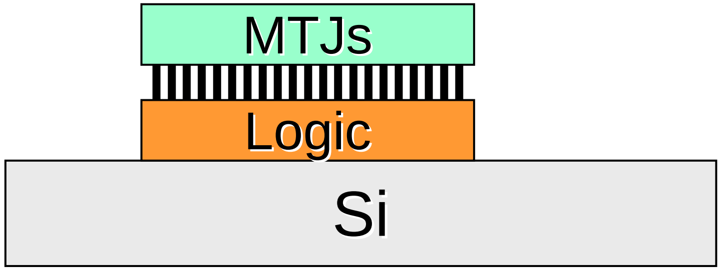


With CMOS technology only:





With hybrid CMOS/magnetic:



Fast communication between logic and memory

-numerous short vias

-simpler interconnecting paths

-Smaller occupancy on wafer

- extended possibilities for programmation and reconfiguration

-possibility to power-off unused CMOS blocks with instant-on restart

New paradigm for architecture of complex electronic circuit (microprocessors...)

Spin-RAM specifications “to be achieved”

	Products / Demos	Predicted	Position vs CMOS
Cell size	20 – 80 F^2	< 10 F^2	>> NAND << SRAM
Technology	Above CMOS		➔ embedded NVM
Speed	~ 40 ns (2.7 ns)	≤ ns ???	~SRAM, µP
Endurance	10^{15}	~ infinite	>> NAND
Non volatility	> 10 years		☺
Scalability	90 nm	20 nm???	???

Logic circuits

- can we make the Spin-RAM to reach high operation speed ?
- at low enough current/voltage compatible with CMOS
- will it be reliable ?

error rate should not be measurable for logic applications

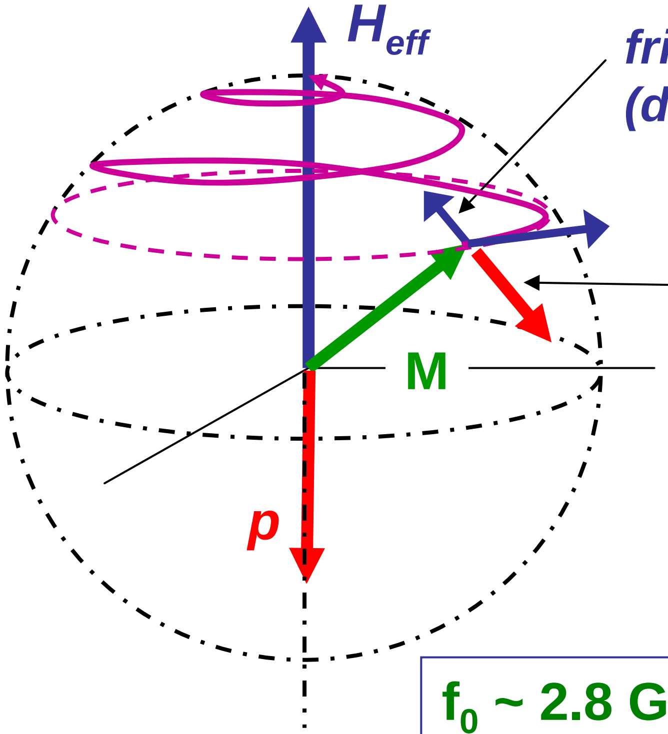
the Landau-Lifshitz-Gilbert (LLG) equation

$$\frac{d\vec{M}}{dt} = -|\gamma|\mu_0\left(\vec{M}\times\vec{H}_{eff}\right) + \frac{\alpha}{\|\vec{M}\|}\left(\vec{M}\times\frac{d\vec{M}}{dt}\right)$$

+ the "spin transfer torque"

$$-G\, j\, \vec{M}\times\left(\vec{M}\times\vec{p}\right)$$

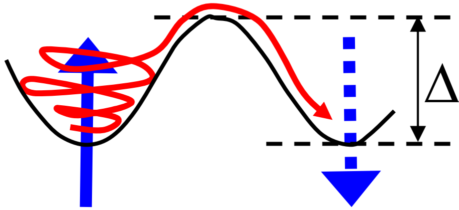
≠ 0 only if *M* and *p* are non colinear



"negative friction" torque induced by spin transfer

f_0 ~ 2.8 GHz / kOe

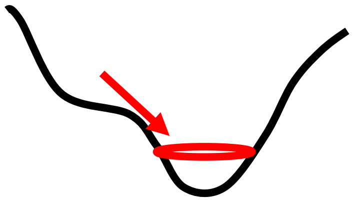
switching threshold J_c :
~ when negative friction overcomes damping



$$\Delta E = KV$$

Thermal stability of storage

ex: stability on 10 years with error rate 10^{-9} ➔ $KV \sim 68\ k_B T$

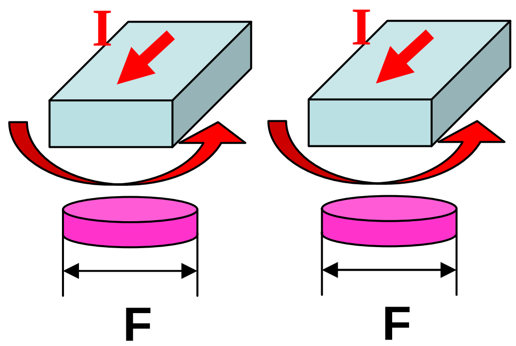


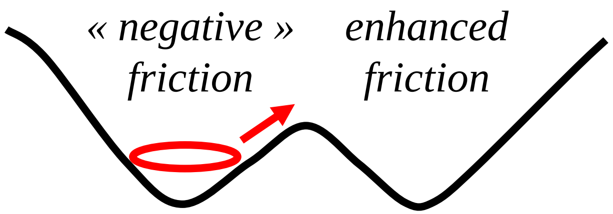
Switching by application of a magnetic field:

(product 2006 by Freescale / Everspin)

fast, deterministic,

… but not scalable





Switching by spin momentum transfer torque:

current below threshold ($J < J_c$) ➔

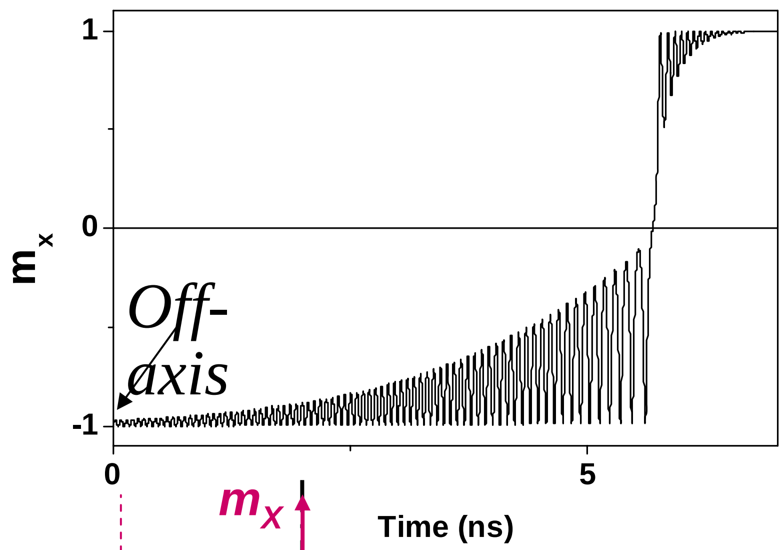
switching controlled by a "gradient of friction »

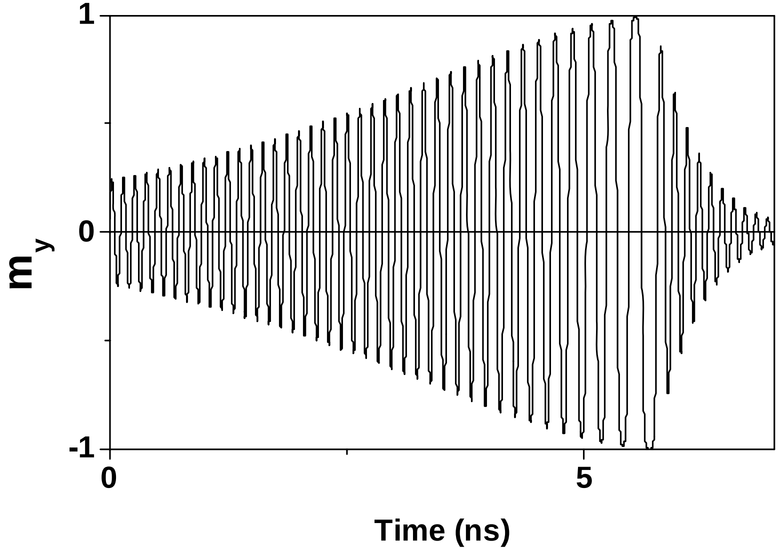
➔ Thermally assisted spin transfer switching :

- **$J \sim J_C$**
- **$t_{pulse} \sim$ 10 – 60 ns** (cf demos Spin-RAM)

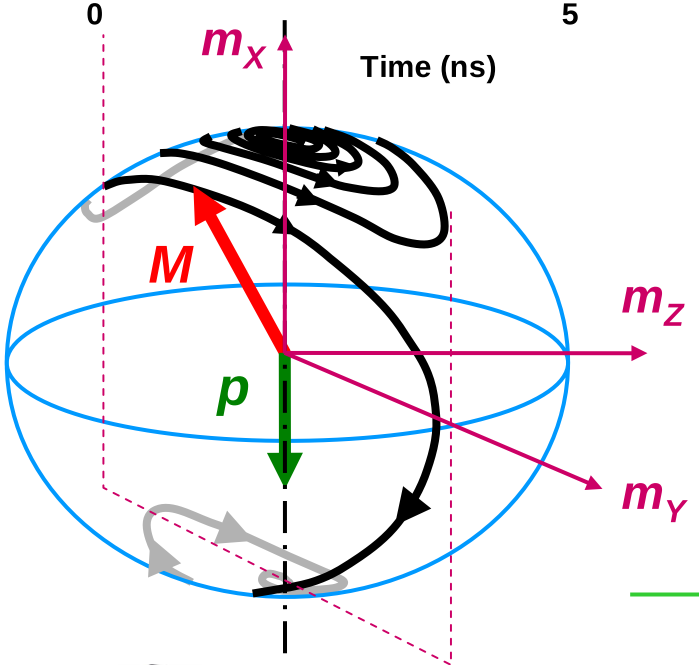
Ultrafast spin transfer switching: basic expectations

Macrospin, T=0K, $J \geq J_{C0}$

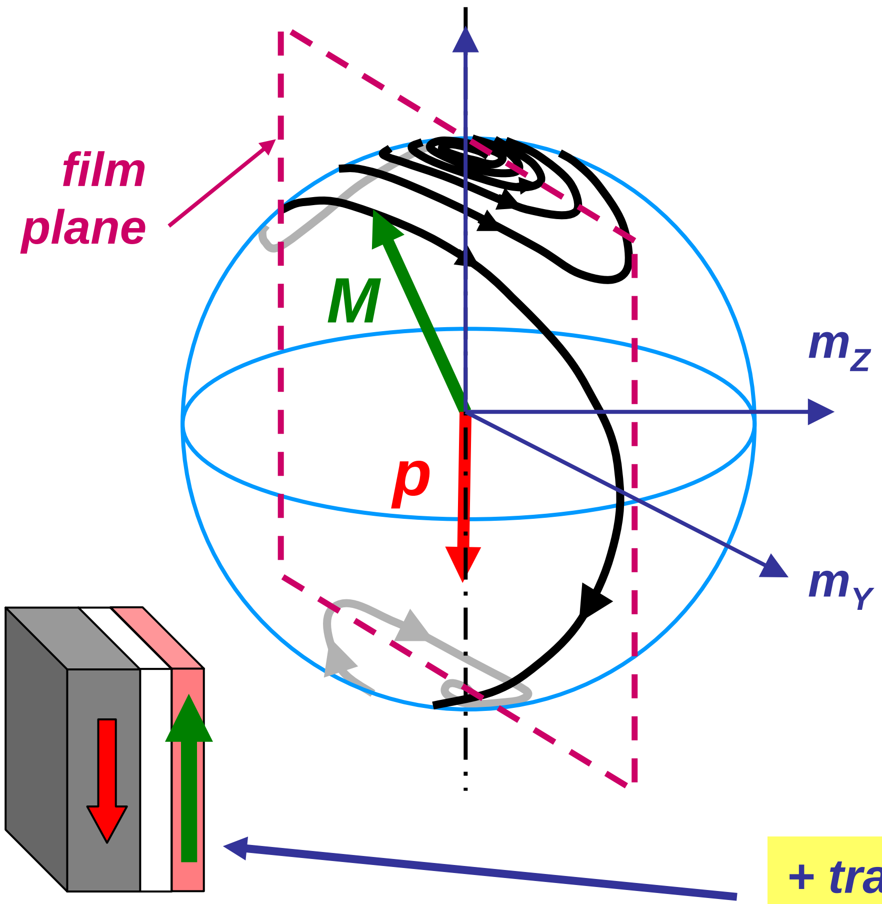




J. Sun, PRB 2000



<u>The case of a platelet magnetized in plane:</u> J.Sun, PRB 62, 570 (2000)



building up precession from an initial orientation θ_0 of *M* :

$$\tau_{WR} \approx \frac{2}{\alpha\gamma_0 M_S}\,\frac{I_{SW}}{\left(I_{pulse}-I_{SW}\right)}\,\ln\left(\frac{\pi}{2\theta_0}\right)$$

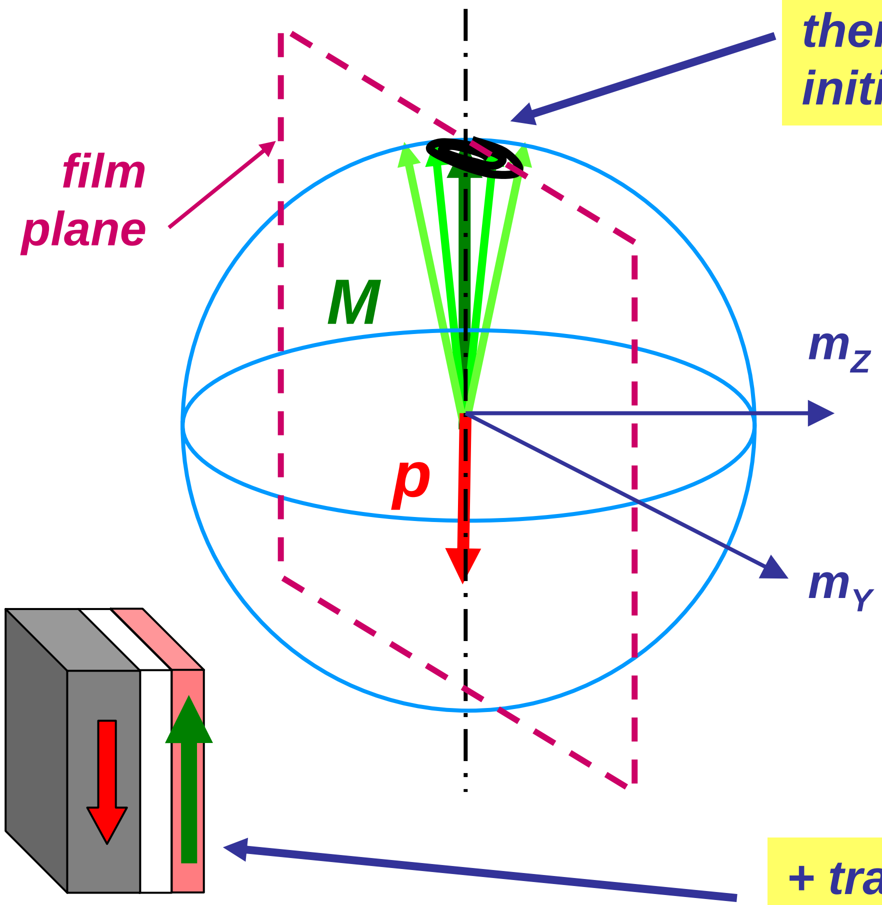
"switching threshold" I_{SW}

fast switching requires currents >> I_{SW}

+ trajectory ~ confined around the plane by dipolar shape anisotropy

Speed: macrospin dynamics of spin transfer writing

The case of a platelet magnetized in plane: J.Sun, PRB 62, 570 (2000)



thermal excitation spreads the initial orientation

+ $$- G\ j\ \vec{M} \times \left(\vec{M} \times \vec{p}\right)$$

= 0 if *M* and *p* are colinear

wide distribution of switching time

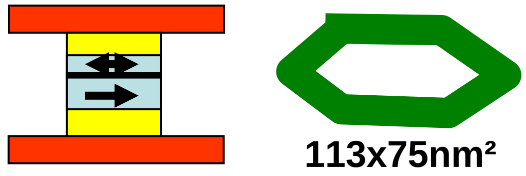
Devolder et al., PRB75, 64402 (2007)

+ trajectory ~ confined around the plane by dipolar shape anisotropy

Switching probability under application of a current pulse

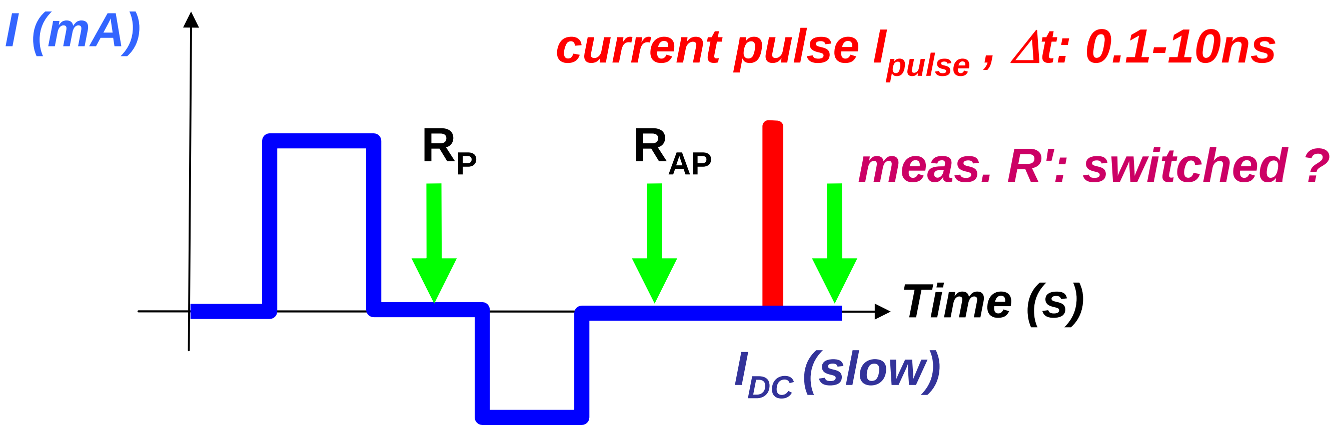
<u>1 – samples:</u> spin valve Nanopillars

J. Katine & M. Carrey, HGST San José



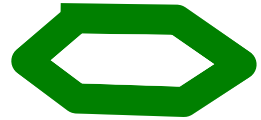
- **PtMn17.5/CoFe1.8/Ru0.8/CoFe2/Cu3.5/CoFe1/NiFe1.8 (nm)**
- **GMR~1.5%**

<u>2 - experiment :</u> **send a series of same current pulses and measures the switching probablility**



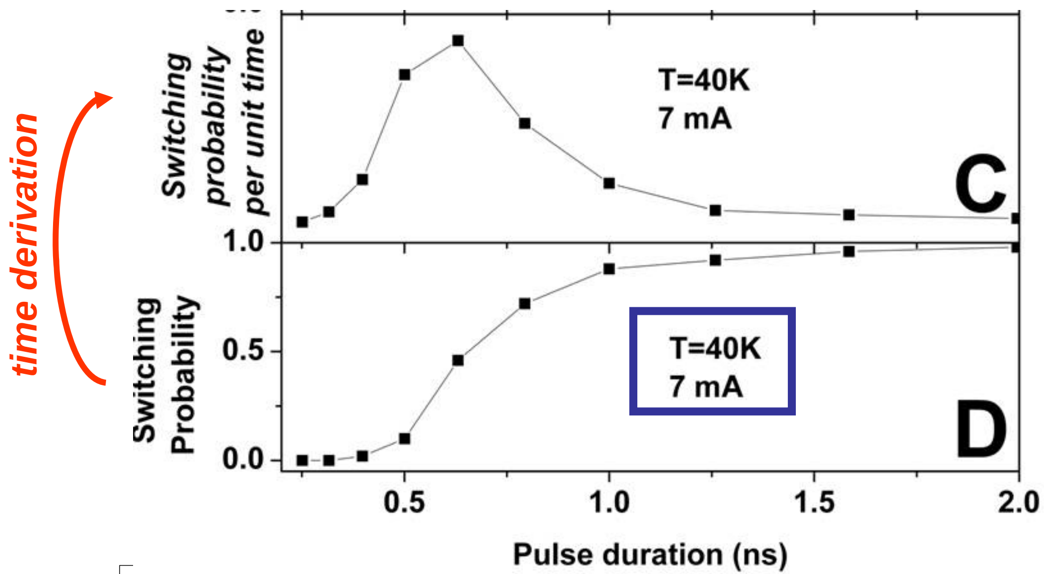
Devolder et al., APL 88, 2006

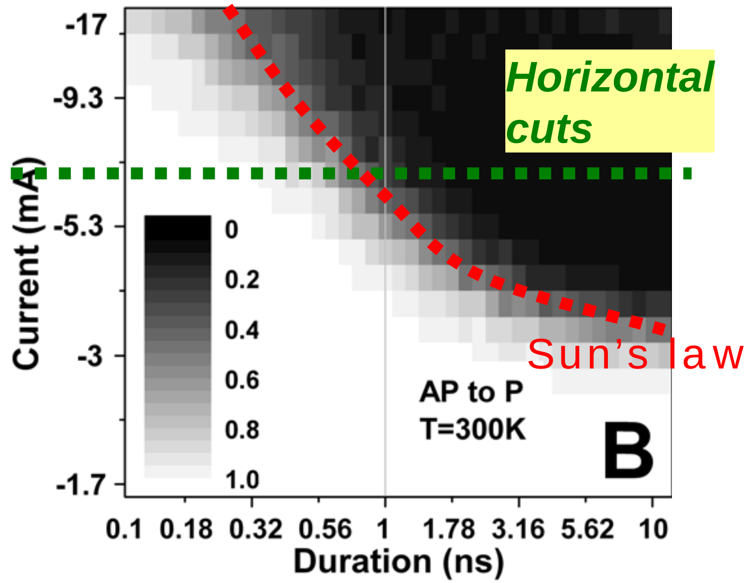
Switching probability versus pulse parameters: (δt, I_{MAX}) in a spin valve nanopillar

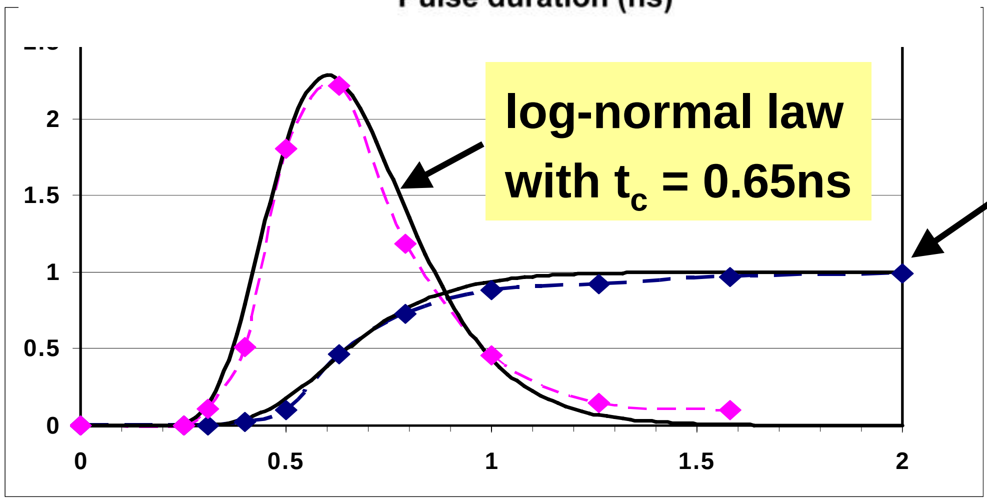


113x75nm²

Devolder et al., APL 88, 2006







error function:

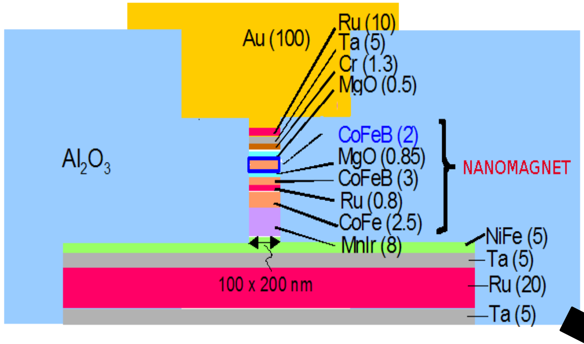
bit error rate < 10^{-9}

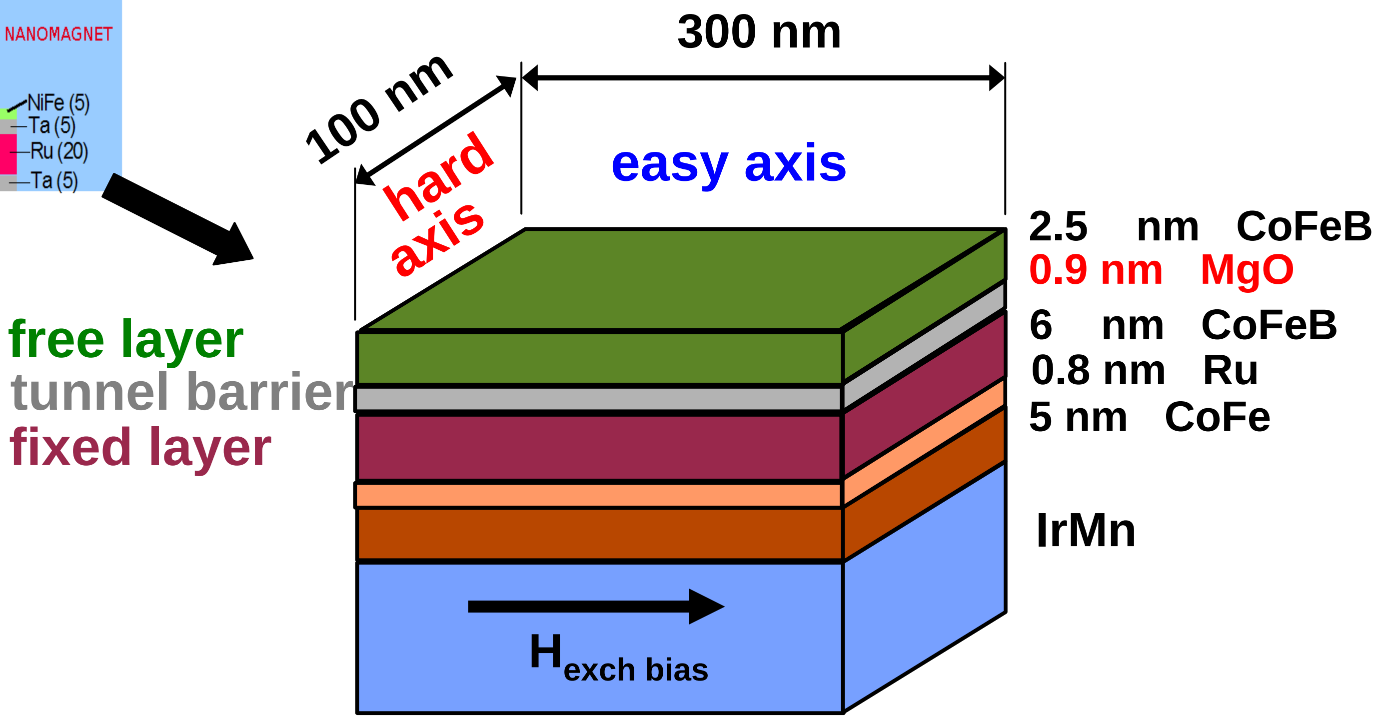
➔ $t_{pulse} > 5\ t_c$

not so fast !!!!!
... for $J > 2\ J_C$

AP➔ P ; H=0

J. Hayakawa et al., Jap. JAP 44, L1267 (2005)

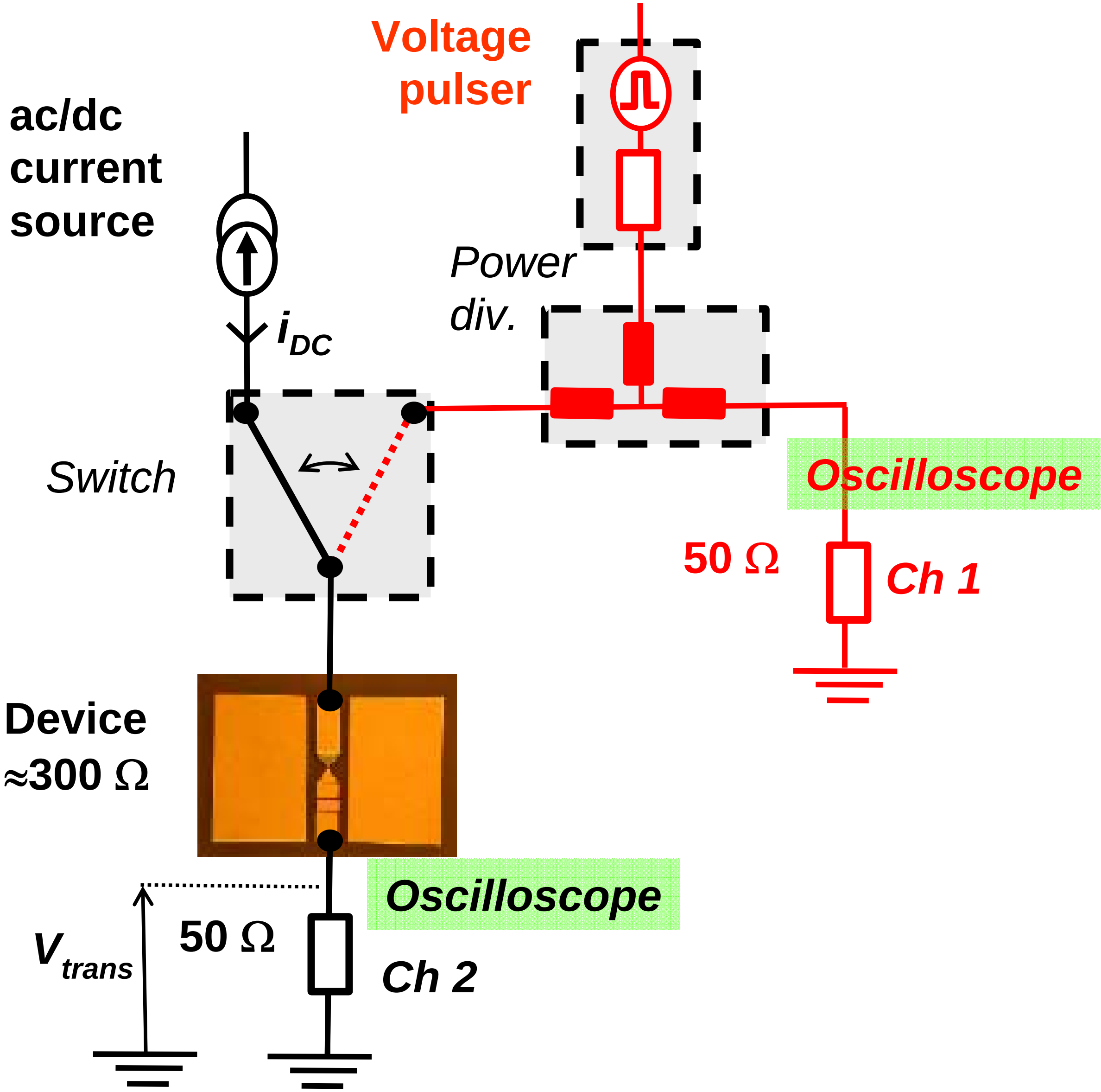


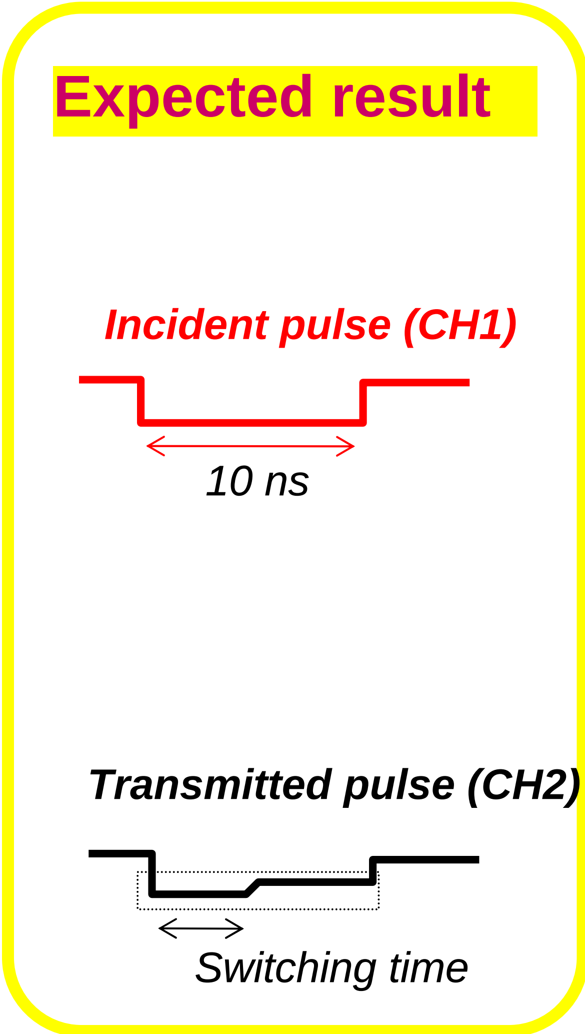


TMR ~ 30 %

➔ single shot measurement are possible

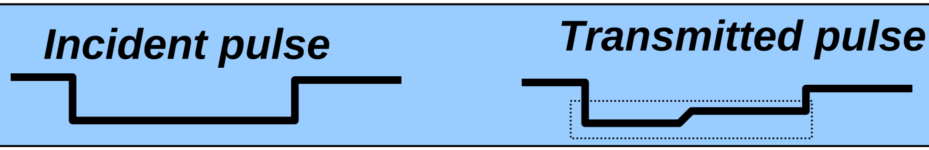
Set-up (complete with HF)

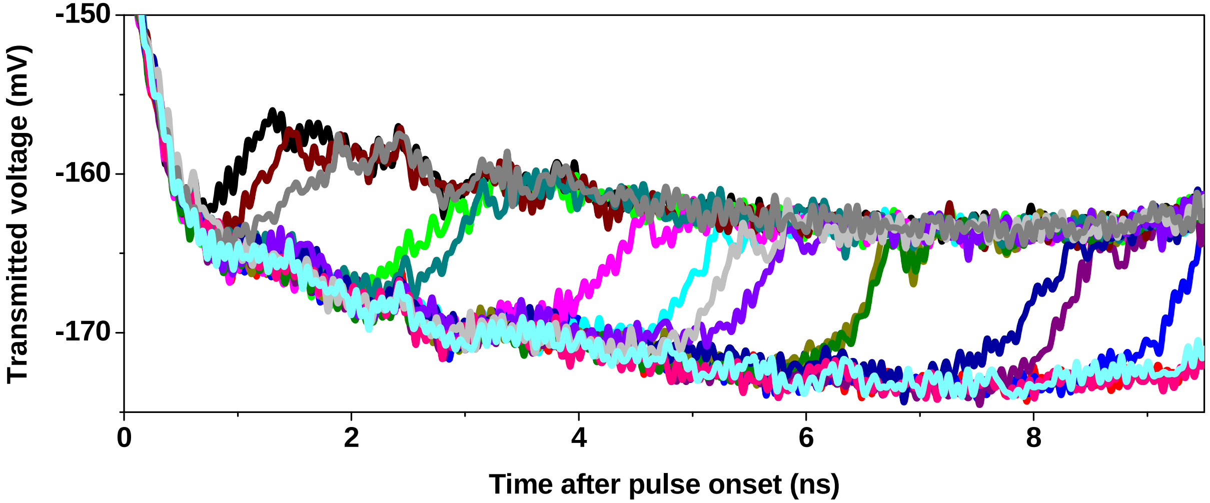




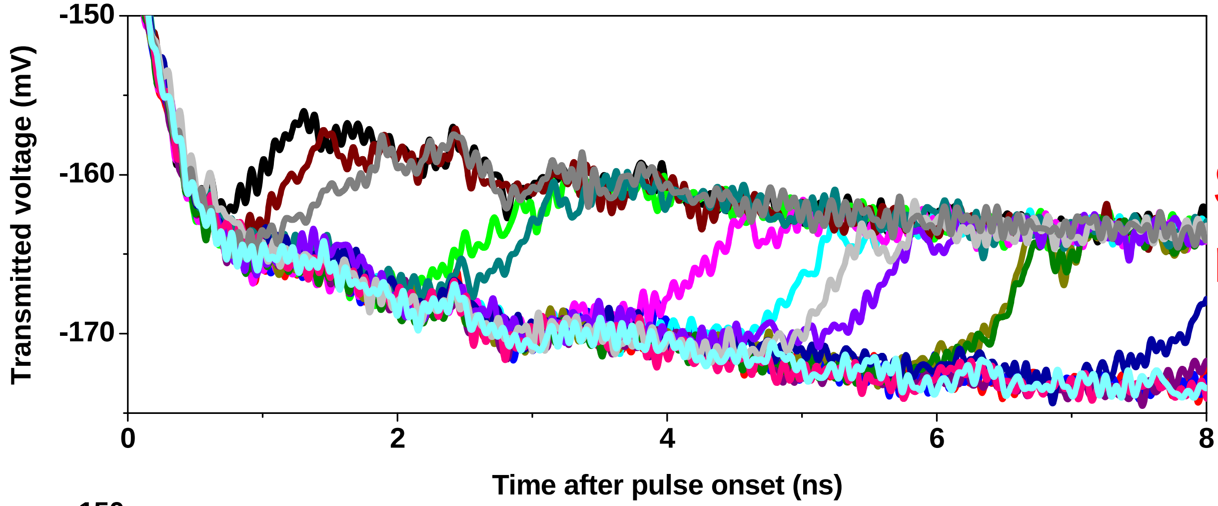
Sample response to a repetition of the same pulse (one color per pulse)

Expected result:

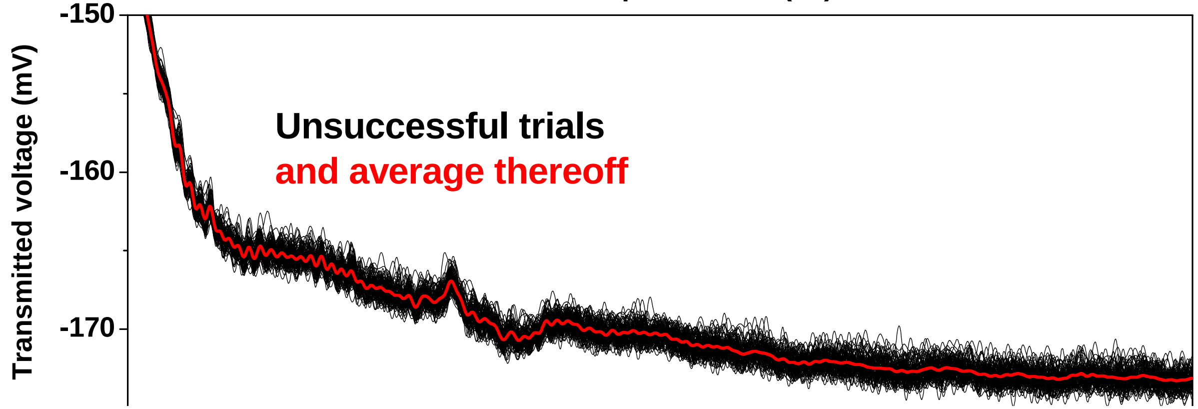




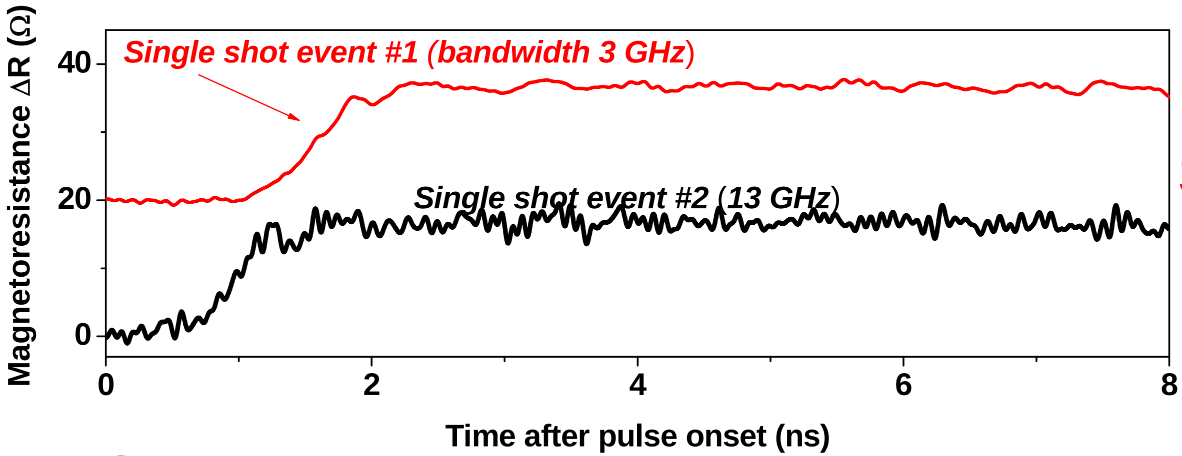
SINGLE-SHOT (time-resolved)



SINGLE-SHOT reversal attempts

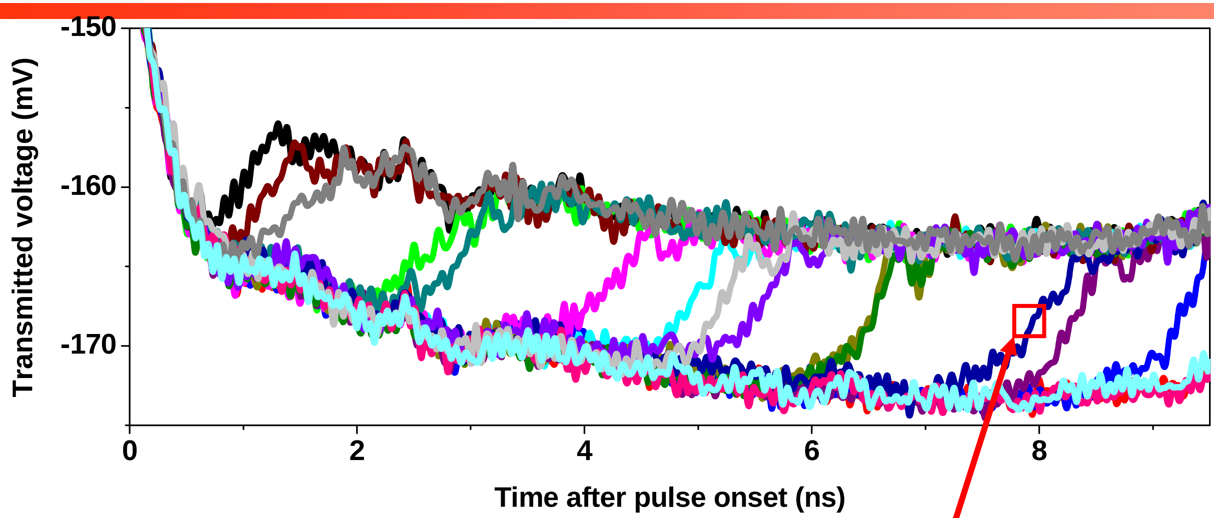


SINGLE-SHOT reversal failures



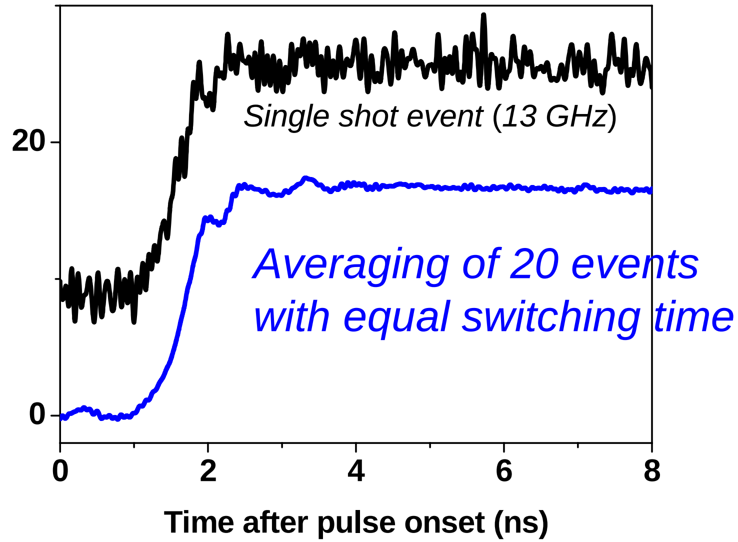
SINGLE-SHOT resistance curves

event-selected-averaged, time-resolved traces



METHOD:
- measure many events
- choose arbitrarily a switching time t_{SW}
- select the events switching at exactly t_{SW}
- average them

=> GET lower noise traces,
MAINTAINING original bandwidth



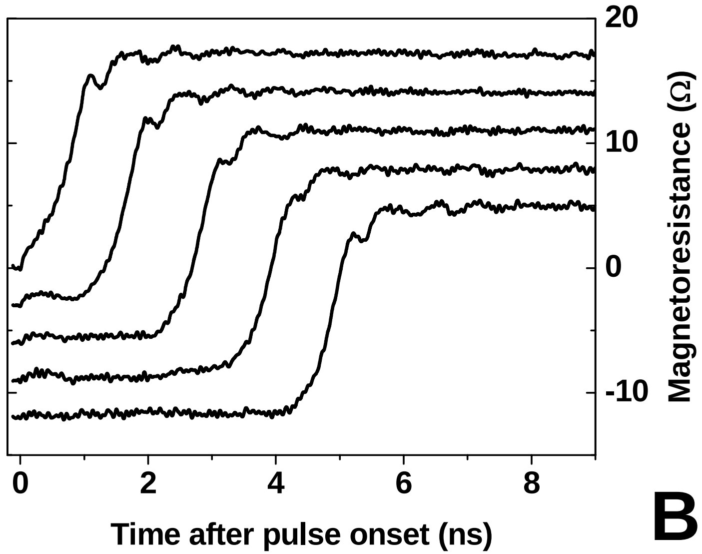
MAIN OUTCOMES:

➔ ***stochastic incubation delay.***

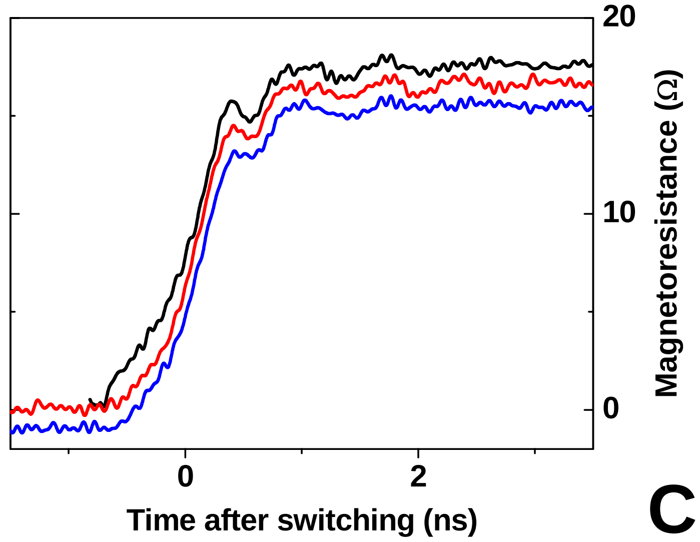
➔ ***then fast switching (~300ps) proceeds through a reproducible trajectory***

➔ ***post-switching ringing: 1.4 GHz, damped in 1.5 ns***

Vertically offset curves



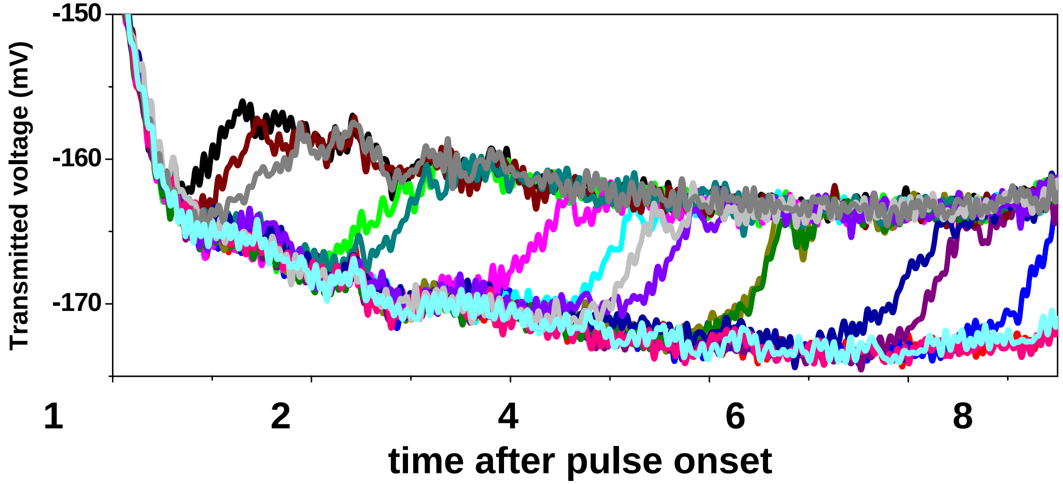
Horizontally offset curves

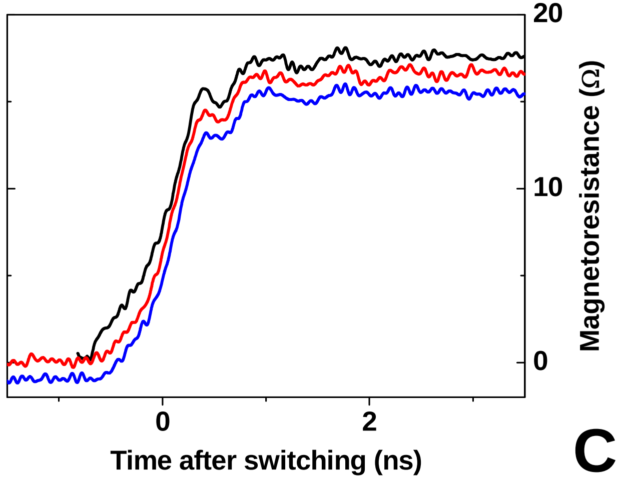


T. Devolder et al, PRL 2008)

Experiment vs macrospin behaviour

Observed:

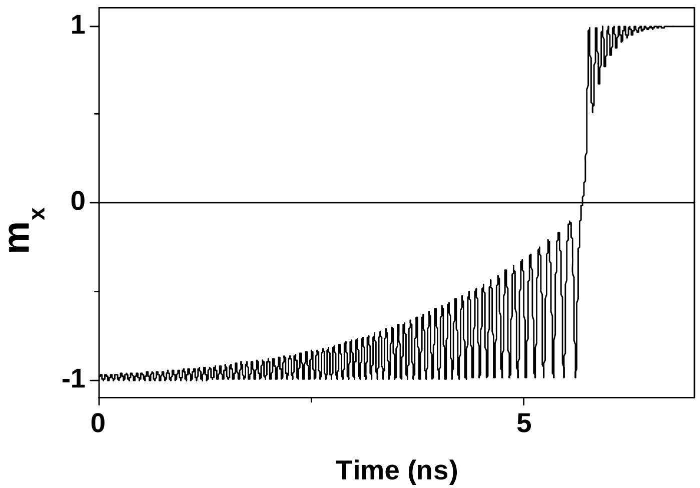




➔ **before switching : random delay + no ringing**

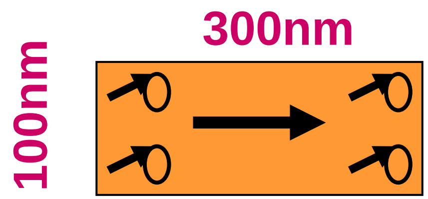
Expected

➔ **build up of oscillating behavior before switching, from a random start due to thermal excitation**



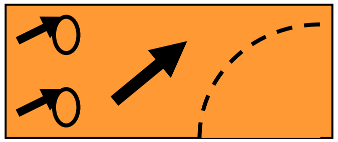
NON UNIFORM SWITCHING

A - stochastic incubation delay



➔ **highly non uniform local excitations**

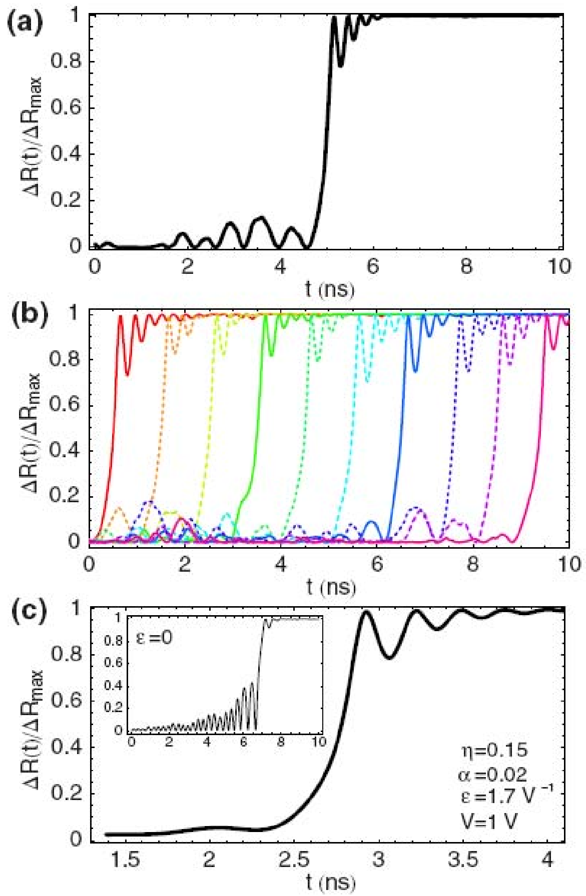
B - fast switching (~300ps) through a reproducible trajectory



C - post-switching ringing: 1.4 GHz, damped in 1.5 ns

MACROSPIN CALCULATION WITH TEMPERATURE AND FILED-LIKE TERM IN SPIN TRANSFER TORQUE

$$\tau = a_J \mathbf{M} \times (\mathbf{M} \times \mathbf{m_P}) + b_J \mathbf{M} \times \mathbf{m_P}$$

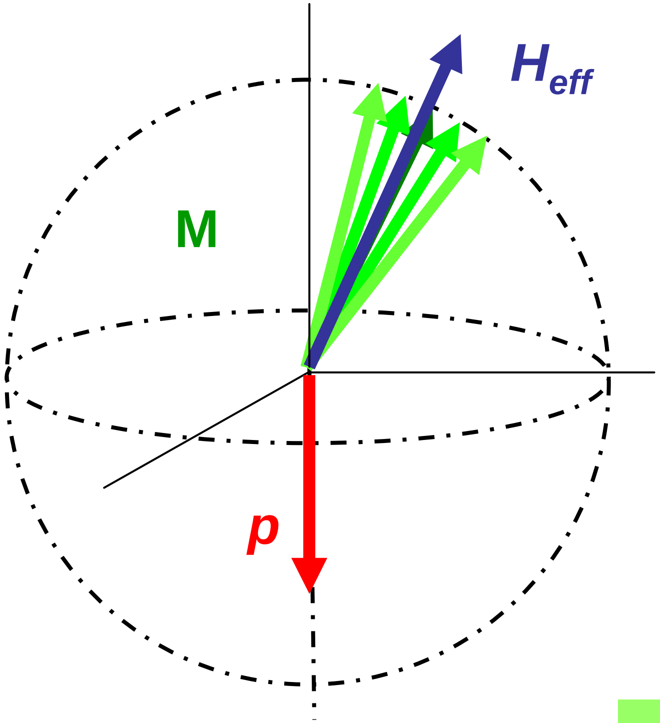


Garzon et al., PRB 2009

Sub-ns switching is possible if we eliminate the initial incoherent stage !

➔ **smaller devices give more coherent behaviour… but still $k_B T$!!!!**

➔ **tilted initial angle between magnetizations of memory and reference layers**



ex: applying a transverse static magnetic field

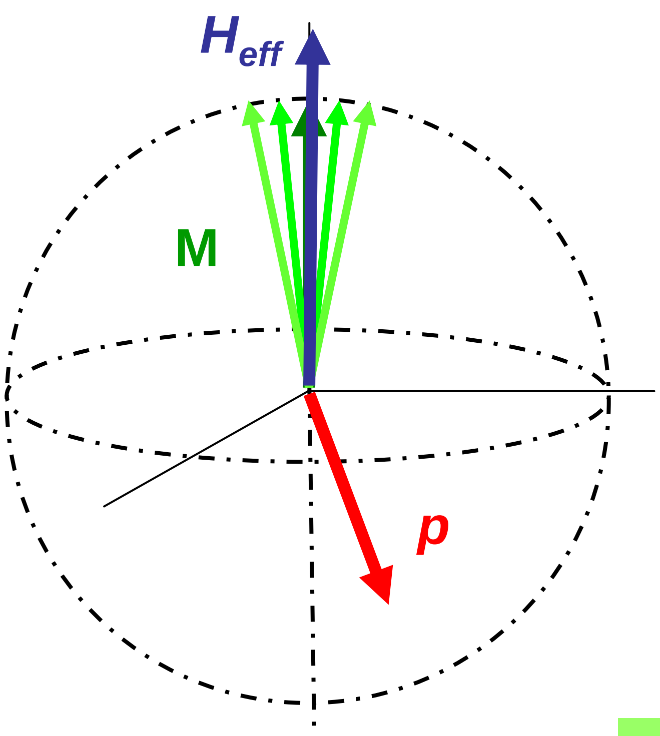
cf: Serrano-Guisan et al., PRL101 (2008) 087201

cf T. Devolder et al., APL 88, 152502 (2006)
+ PRB 75, 064402-1,5 (2007) + PRB 75, 224430-1,10 (2007)

Sub-ns switching is possible if we eliminate the initial incoherent stage !

➔ **smaller devices give more coherent behaviour… but still k_BT !!!!**

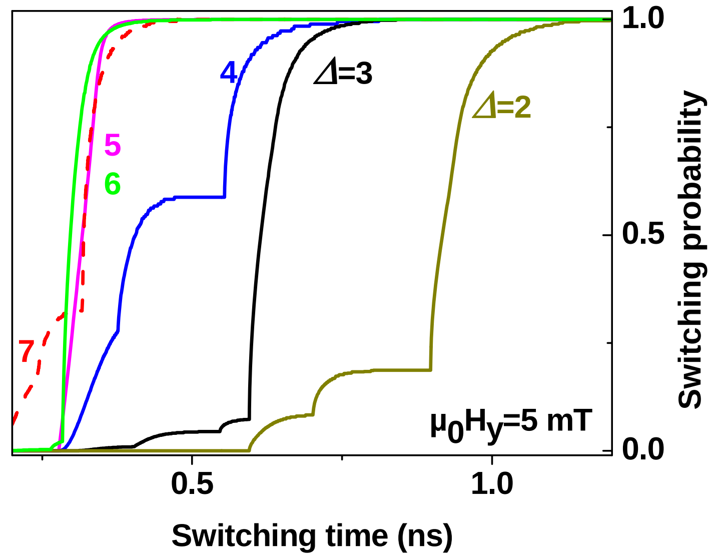
➔ **tilted initial angle between magnetizations of memory and reference layers**



ex: biasing the reference layer at an angle

(cf Krivorotov, Intermag 2008)

our simulations



cf T. Devolder et al., APL 88, 152502 (2006)
+ PRB 75, 064402-1,5 (2007) + PRB 75, 224430-1,10 (2007)

Sub-ns switching is possible if we eliminate the initial incoherent stage !

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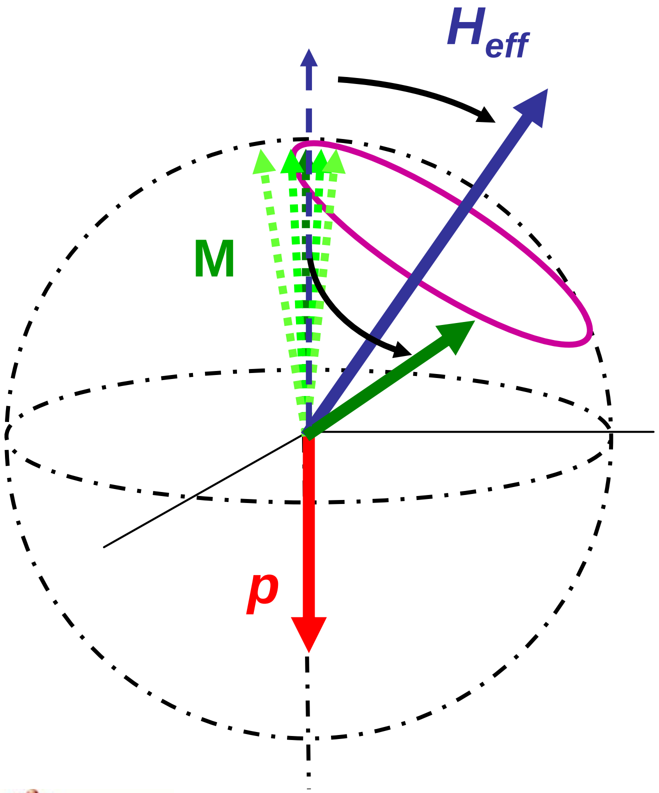
➔ **start a large angle precession at or before current pulse onset**



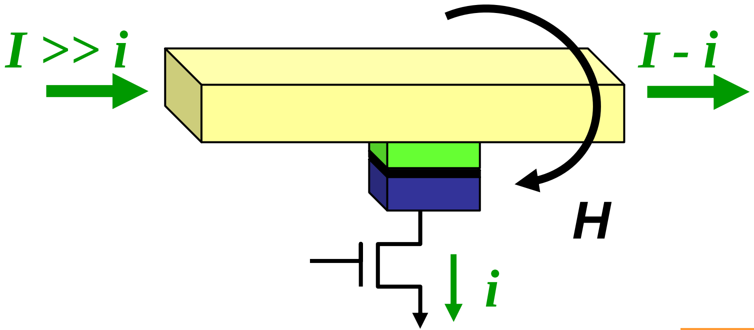
by changing the magnetic energy ➔ H_{eff}

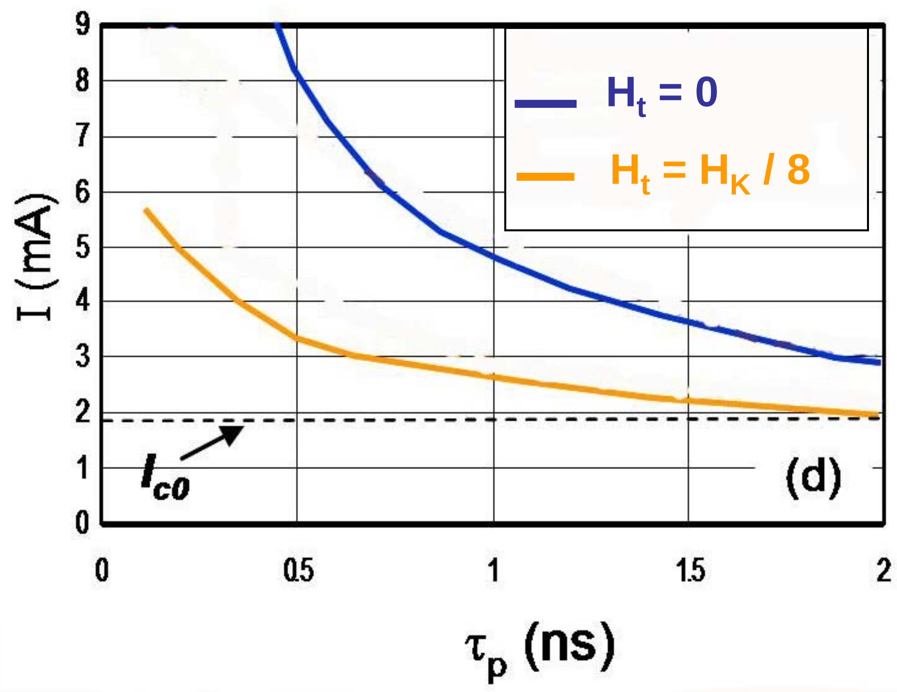
➔ associate synchronous pulses of current *i* and transverse magn. field *H*

Ito et al., APL89, 252509 (2006)

could be intrinsic to cell architecture

W.C. Jeong et al., VLSI 2005





+ allows to reach sub-ns speed at $J \sim J_C$

- more complex cell with applied field

Sub-ns switching is possible if we eliminate the initial incoherent stage !

➔ **smaller devices give more coherent behaviour… but still k_BT !!!!**

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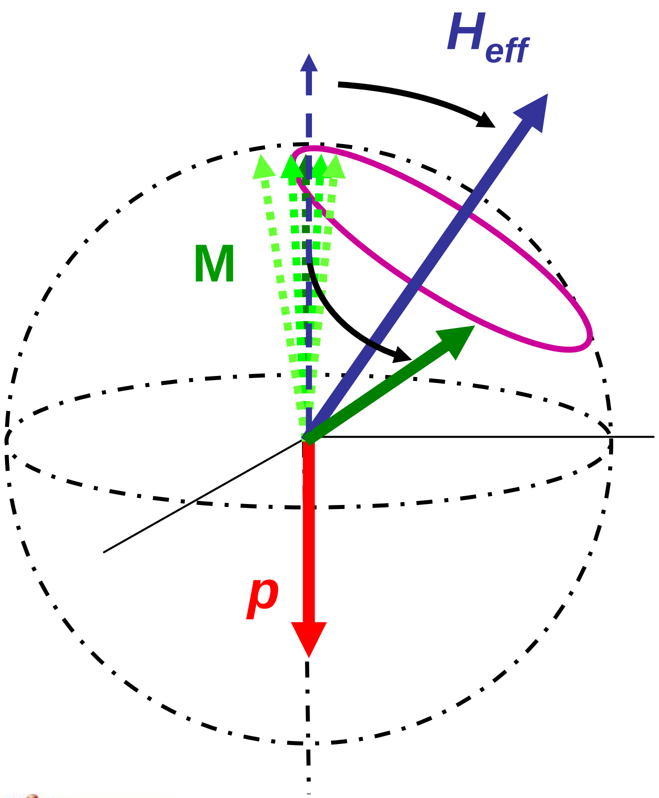
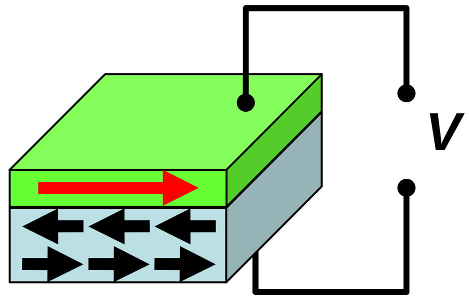


by changing the magnetic energy ➔ H_{eff}

➔ **change the internal effective field !**

ex: coupling to a multiferroic layer + voltage

Ramesh et al. NatMat6, 21 (2007)



Also: strain, cf : Lee et al. APL82 (2003); Boukari et al., JAP 101 (2007) (on metals)

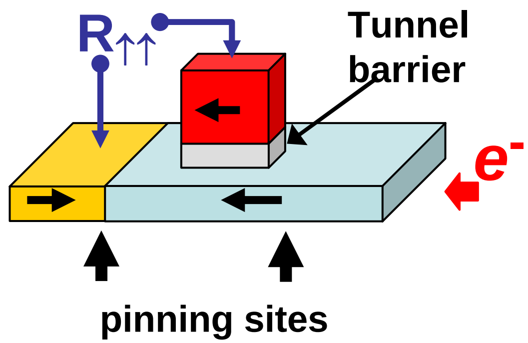
CONCLUSION

- **similar stochastic behaviour for DW depinning by current pulse (*cf Moriya, Nat. Phys. 2008; C. Burrows, Nature Phys. in press,*)**

  ➔ **storage track memory (cf S. Parkin, this conference)**

  ➔ **DW MRAM**

  Fukami et al. (NEC), VLSI 2009



- **critical current for spin transfer switching still needs to be reduced (by 3 o 5) to ensure high density and scalability @ ~10ns R:W cycle**
  ➔ **perp. magnetized materials (*E. Fullerton, this conf.*)**
  ➔ **synthetic antiferromagn. free layer (*Hayakawa, Jpn. J. Appl. Phys 2006*)**

- **speed potential maybe the major asset for MRAM, but assistance to spin transfer should be necessary to reach sub-ns switching**

Ultrafast MRAM for "logic in memory":
a new paradigm for architecture of complex electronic circuit (microprocessors...)

Zhao et al., IEEE Trans Mag. 2009 ; Matsunaga et al., DATE'09)

Thank you for your attention !