Massive fabrication of Single-Walled Carbon Nanotube Field Effect Transistors

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Centre Nacional de Microelectrònica IMB CSIC Consejo Superior de Investigaciones Científicas UAB

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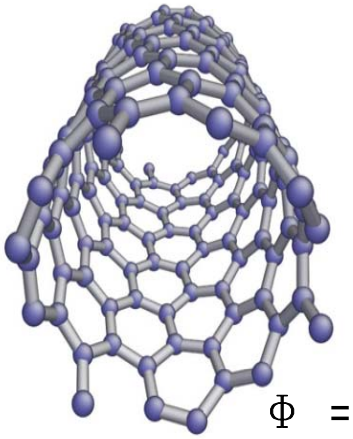
Single-wall carbon nanotube (SWCNT)



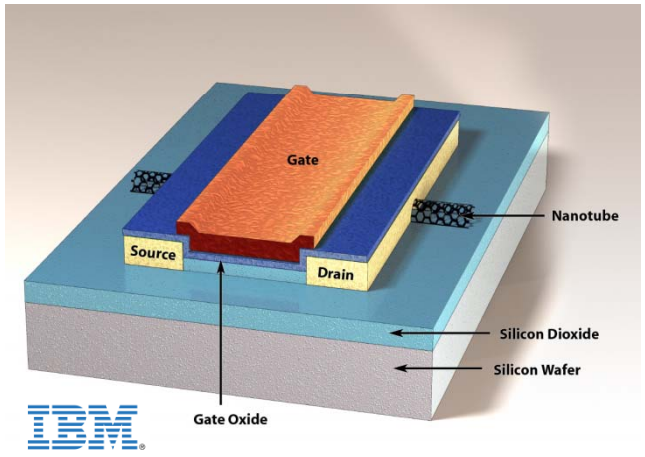
Φ = 0.4 – 2 nm

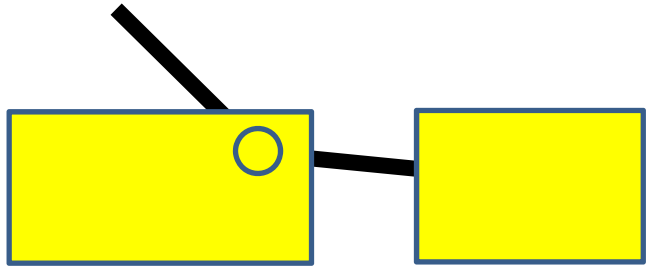
Electrical properties

- ❑ 1D conduction
- ❑ Metallic / Semiconducting (E_g α 1/d)

Mechanical & sensing applications

The single-walled carbon nanotube transistor



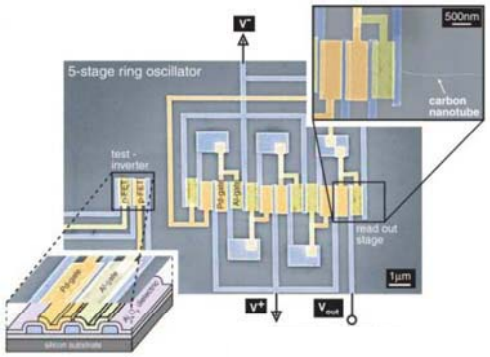


☹ Control over growth direction

☹ Control over chirality

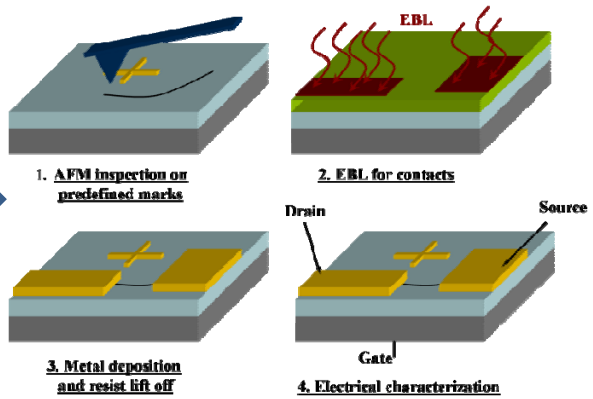
CNT-FET based device fabrication

Discrete fabrication:



Ring oscillator assembled on a SWCNT

Z. Chen et al., Science 311 (2006)

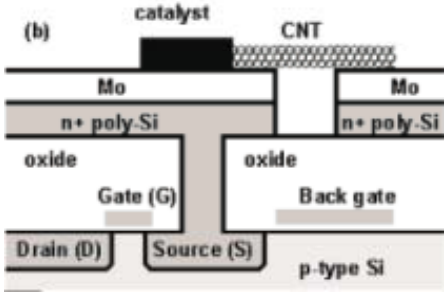


☹ Slow process flow

☹ Low throughput

☹ No statistical data

Batch fabrication:



CNT & CMOS integration:
- 2048 devices/chip
- 1% functional CNT-FET

YC Tseng et al., Nano Letters Vol. 4, No. 1 (2004)

☺ Batch fabrication

☺ Wafer scale fabrication

☺ Statistical data

☹ Few published works

☹ Statistics on not more than some hundreds of devices

OBJECTIVE

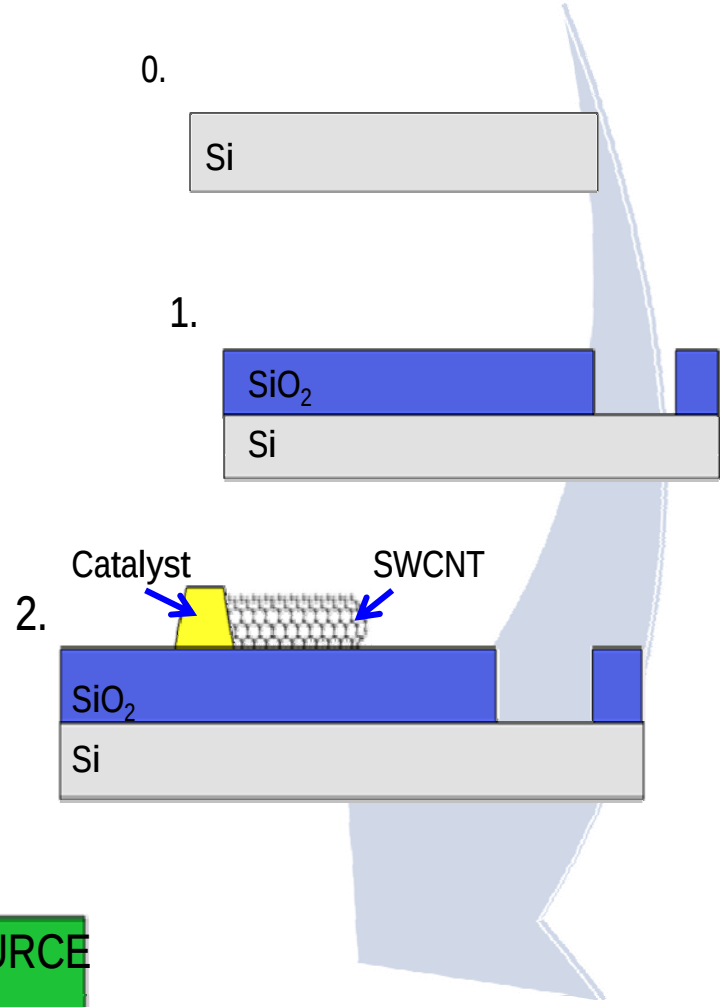
Develop the technology for batch fabrication and testing of CNT-FET based systems.

- **Technology for batch fabrication of CNT-FET structures at 4 inch wafer scale**
- **Procedure to evaluate the resulting CNT-FET structures**

Technological process

- 15 microelectronics standard steps
- 3 Photolithographic processes

0. Si 4” wafer
1. Back gate contact
2. SWCNT selective synthesis
3. Contact patterning



CNT-FET structure design

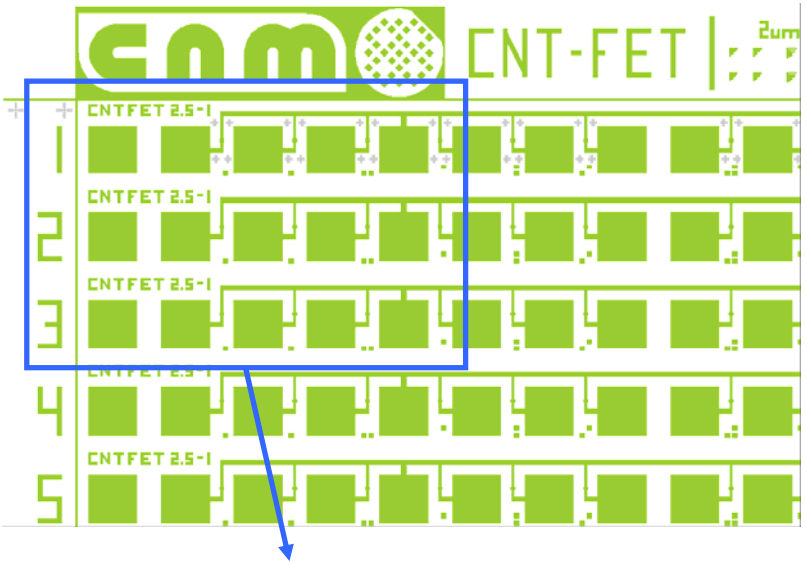
Chips de 15 x 15 mm^2

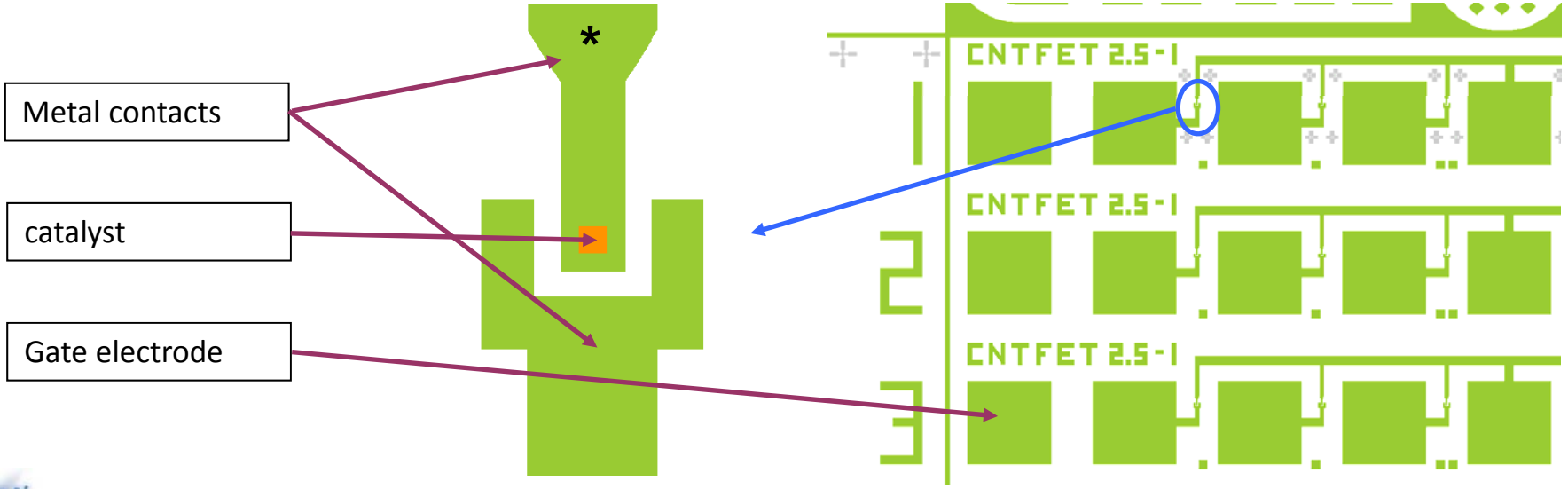
5,760 $^{device}/_{chip}$, 360 $^{geometry}/_{chip}$

→ 2,560 devices/cm^2

16 geometries

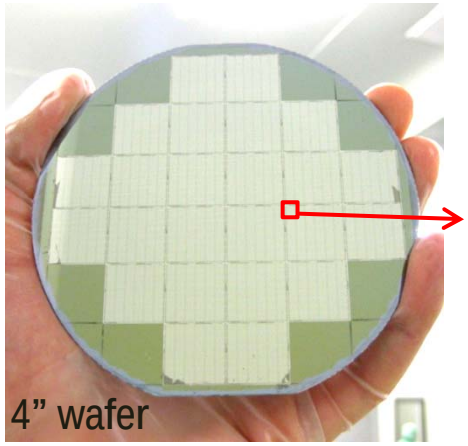
- Catalyst area: 1x1 / 2x2 / 4x4 / 5x5 μm^2
- Channel: 1 / 3 / 5 / 7 µm

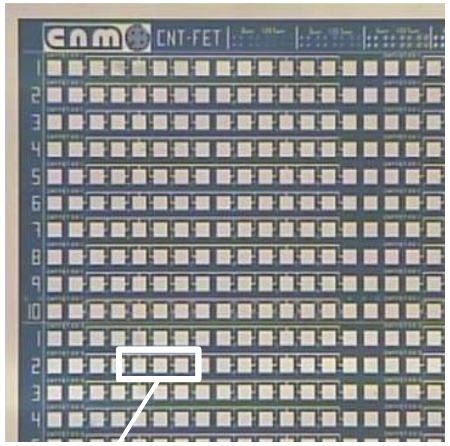


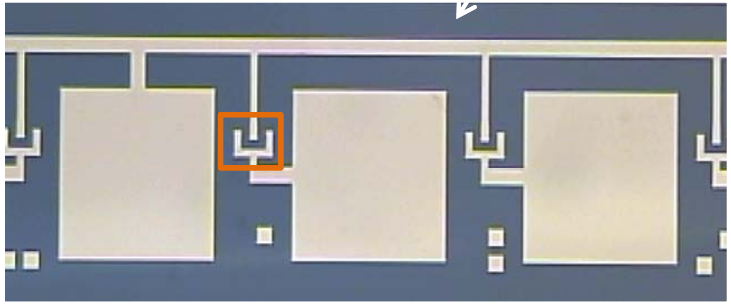


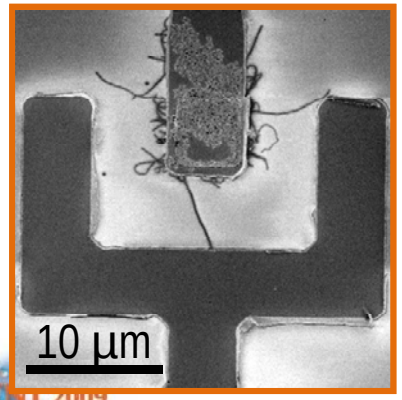
* YC Tseng et al., Nano Letters Vol. 6, No. 7 (2006)

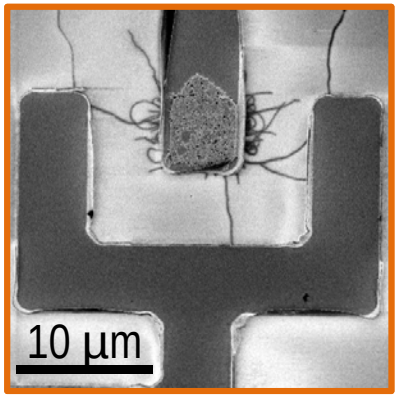
CNT-FET fabrication results











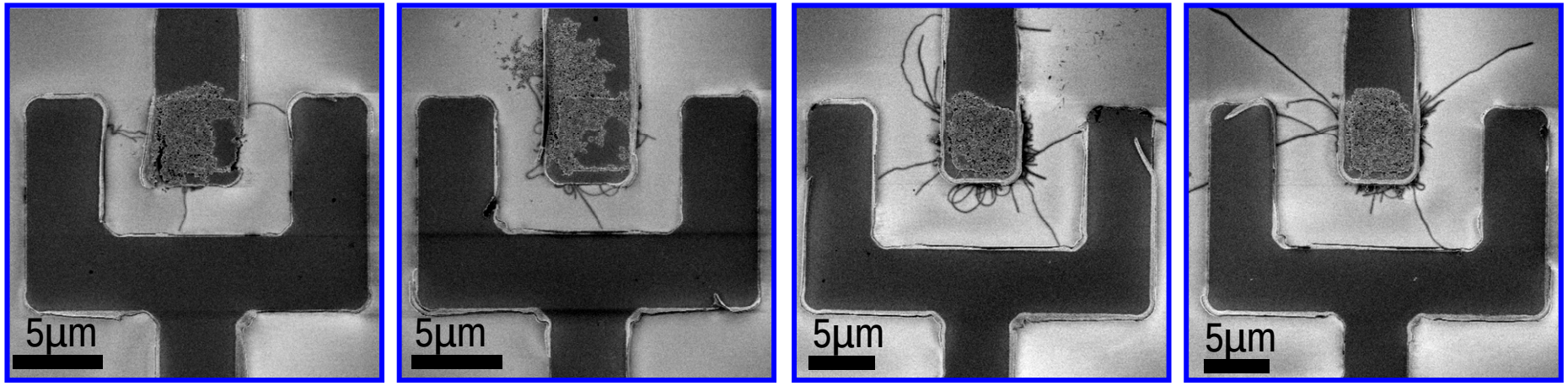
Structure fabrication:

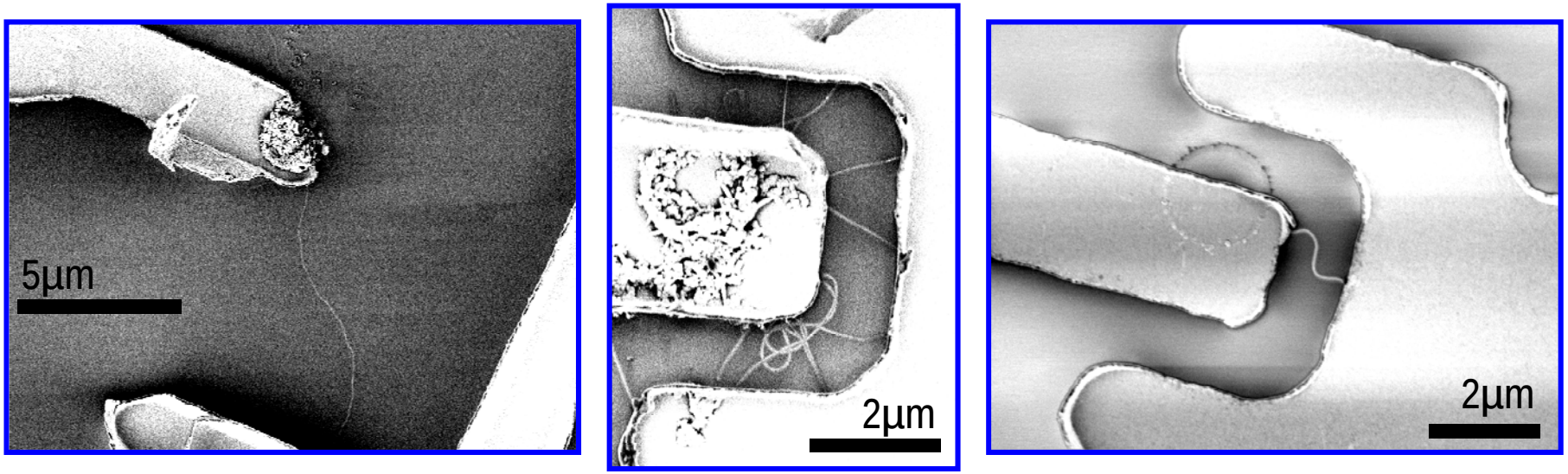
- ❑ Batch fabrication (4” wafer scale)
- ❑ 5,760 dev./chip x 24 chip/wafer

  ~140,000 dev./wafer

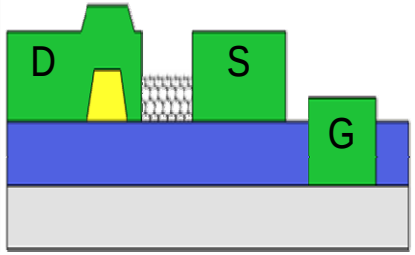
Nanotubes:

- ❑ Localised growth of SWCNTs at 4” wafer scale
- ❑ Diameter: < 2nm → SWCNTs
- ❑ Length: ~ 1-10 µm
- ❑ Density: 0.5 SWCNT/µm^2

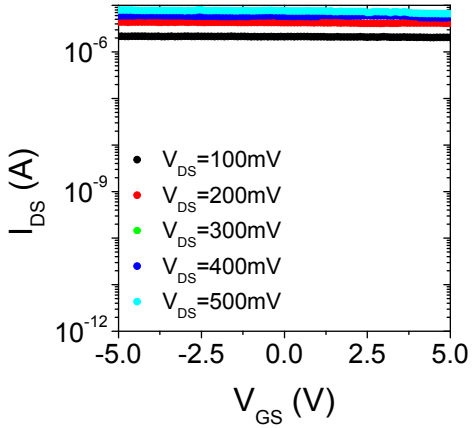

5µm
5µm
5µm
5µm


5µm
2µm
2µm

I/V characteristics of operative structures



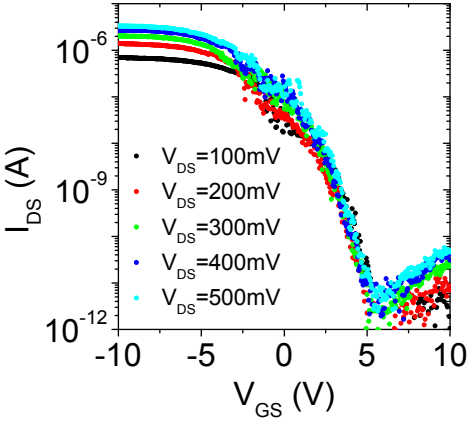
Metallic SWCNT:



$I_{DS} \neq I_{DS}(V_{GS})$

$I_{DS} \approx 10^{-6}$ A

Semiconducting SWCNT:



P-type

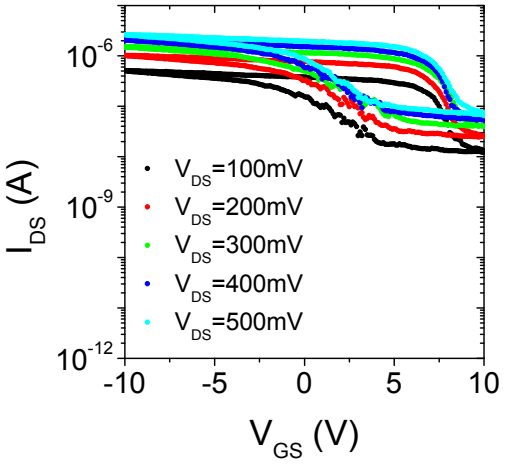
$I_{DS} = I_{DS}(V_{GS})$

- $I_{ON} \approx 10^{-6}$ A
- $I_{OFF} \approx 10^{-12}$ A

Functional CNT-FET:

$I_{ON}/I_{OFF} \geq 100$

Semiconducting + metallic SWCNT



More than one contacted CNT

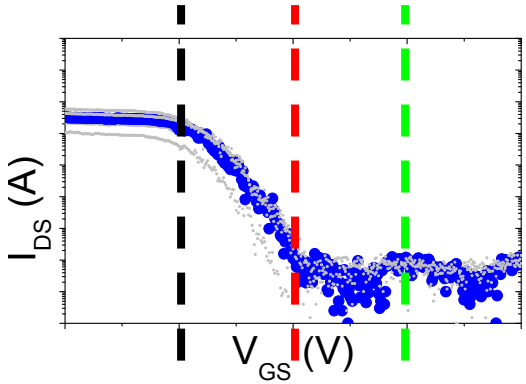
$I_{DS} = I_{DS}(V_{GS})$

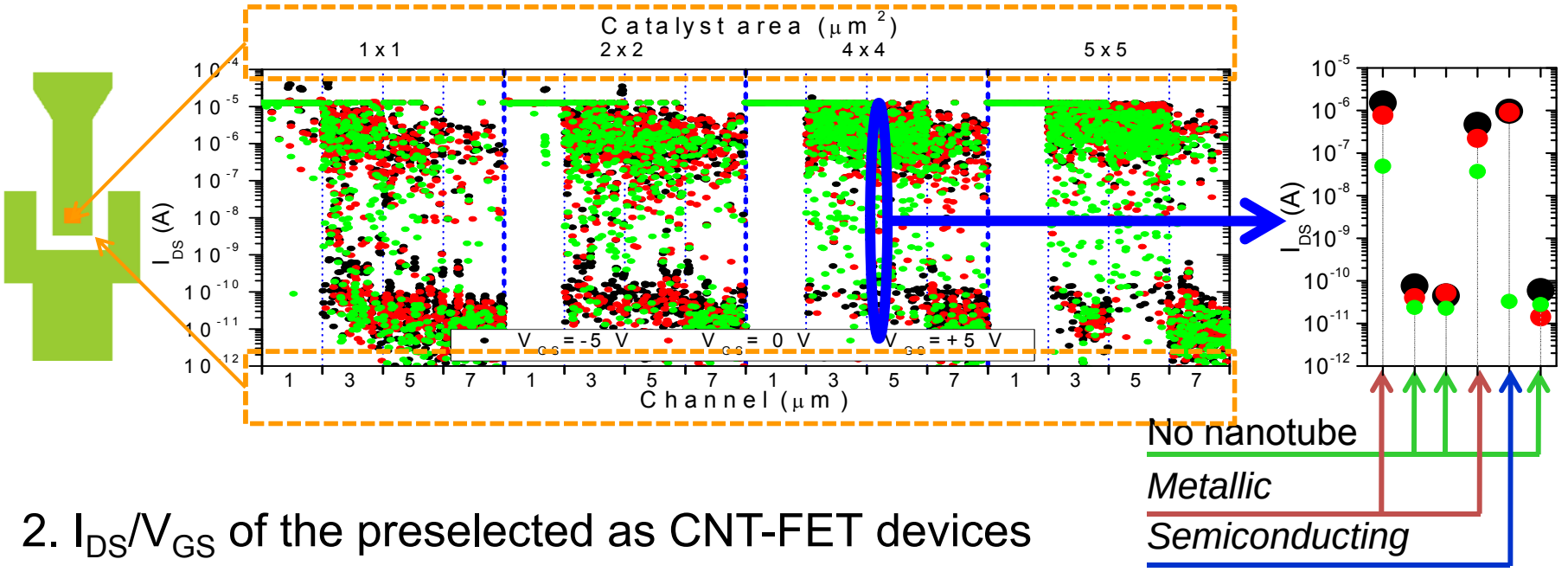
- $I_{ON} \approx 10^{-6}$ A
- $I_{ON}/I_{OFF} < 100$

3 point automatic testing of CNT-FET structures

1.Batch 3 I_{DS} per structure

- $I_1=I_{DS(VGS=-5V)}$
- $I_2=I_{DS(VGS=0V)}$
- $I_3=I_{DS(VGS=+5V)}$

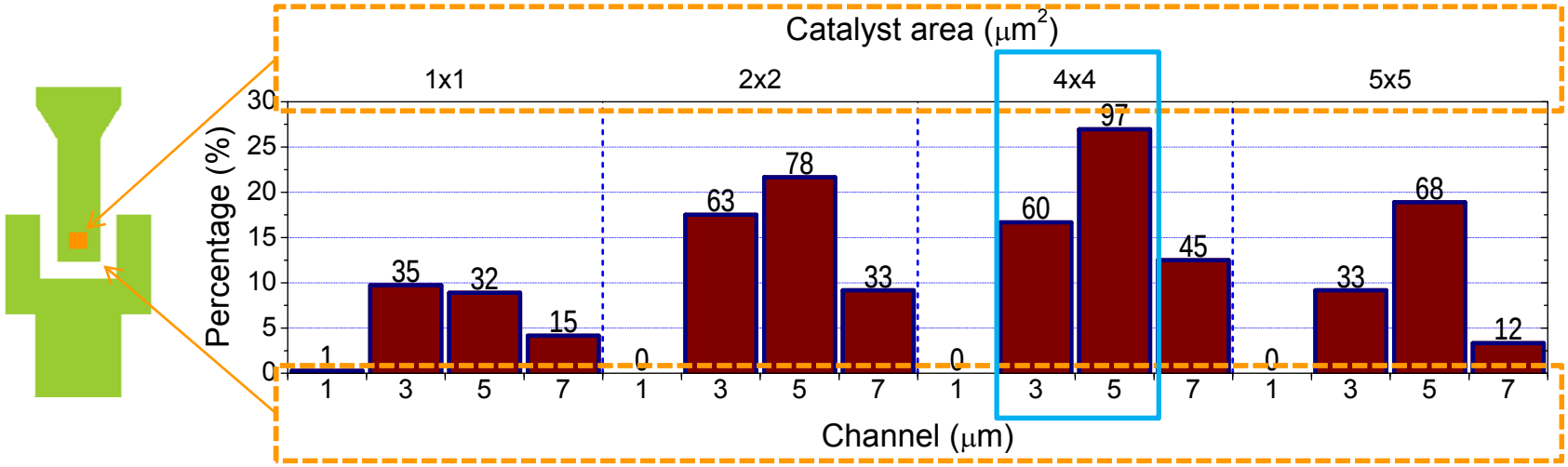




2. I_{DS}/V_{GS} of the preselected as CNT-FET devices

More than 100 structures have been tested to validate the procedure

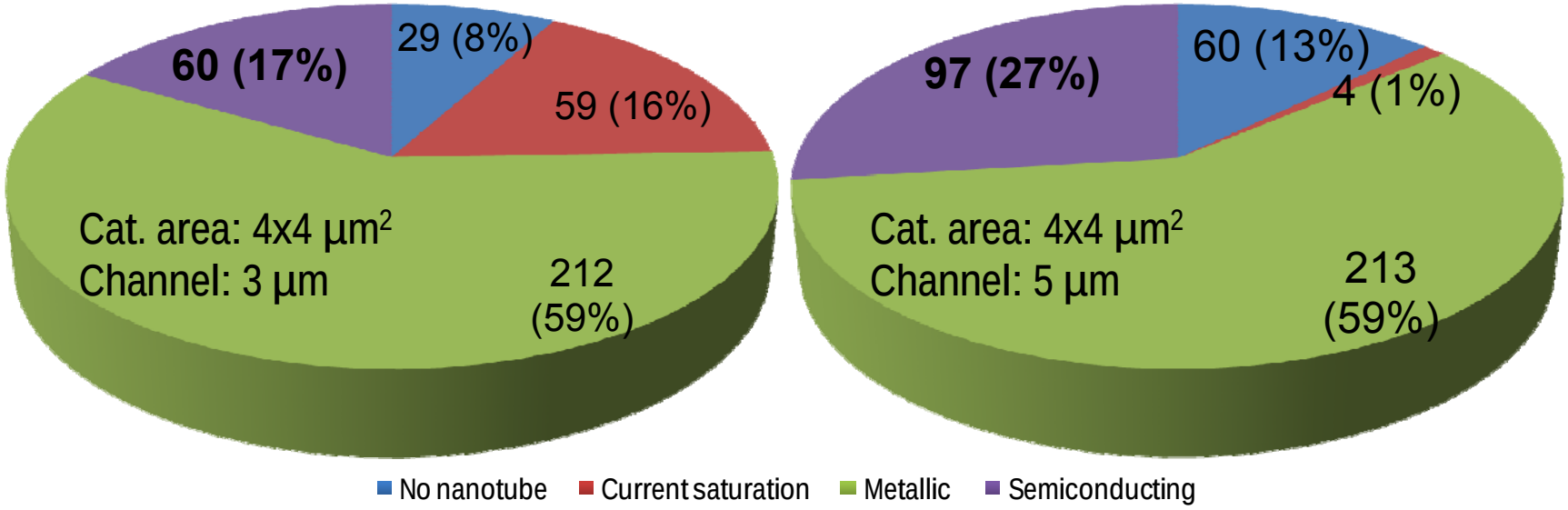
Statistical analysis of functional transistors on CHIP16



- 97 (27 %) functional CNT-FET for the 4x4 μm² and 5 μm design.
- 572 (10%) functional transistors in one 15x15 mm² chip.

- 4x4 μm² is the catalyst area for the most functional CNT-FET.
- 5 μm is the gap for the most functional CNT-FET.

Comparison between 3µm and 5µm channel CNT-FET



When channel increases:

→ Increase of “no nanotube” devices

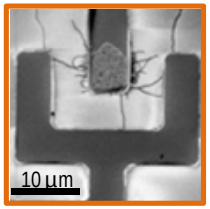
→ Decrease of “current saturated” devices

→ Increase of functional CNT-FET

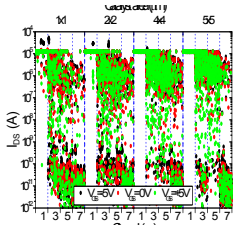
a. less defective fabrication

b. less of probability of more than one SWCNT being contacted

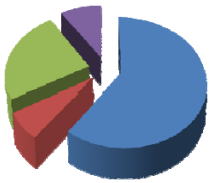
Summary



- Massive batch fabrication of CNT-FET at 4” wafer scale has been demonstrated.



- A procedure for automatic testing of very high number of CNT-FET structures has been presented.
- CNT synthesis, device fabrication and CNT-FET characteristics may be evaluated.

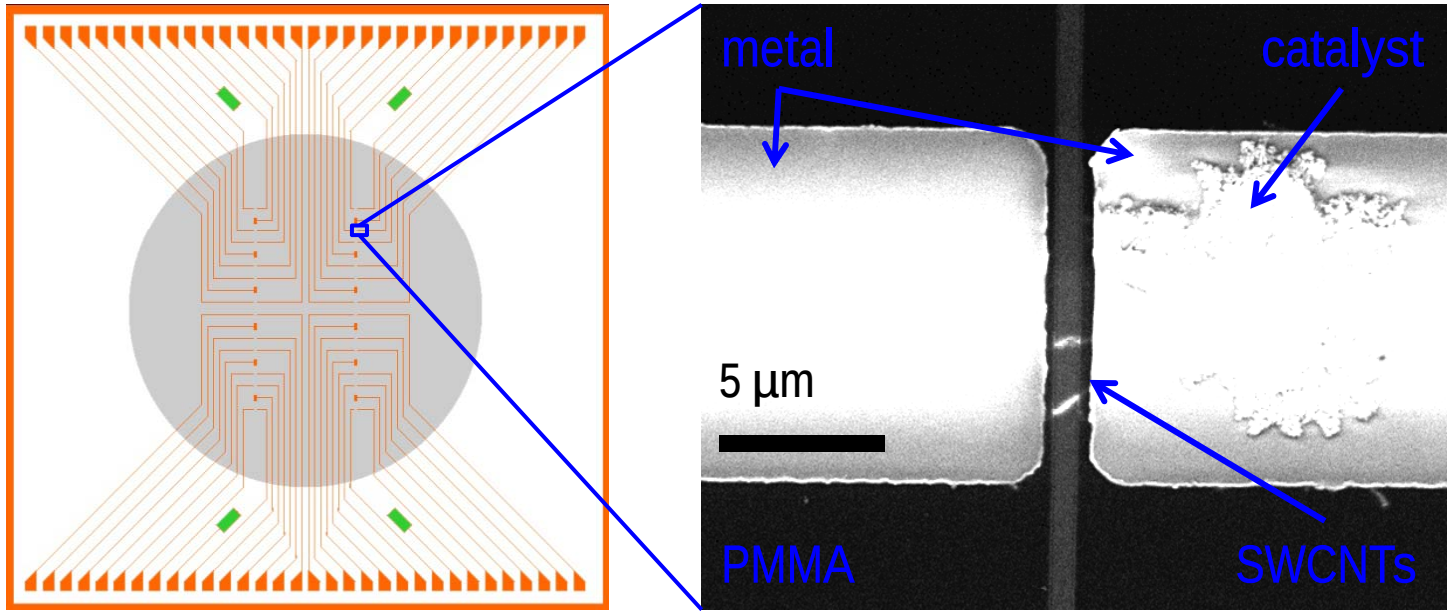


- 10,000 functional CNT-FET have been fabricated on a 4” wafer.
- Up to 27 % success functional CNT-FET fabrication for certain designs (4x4 μm^2 & 5 µm and 5x5 μm^2 & 7 µm)

Prospective

- Optimization of design and process flow.
- New analyses to evaluate the devices such as SWCNT density per device or CNT diameter

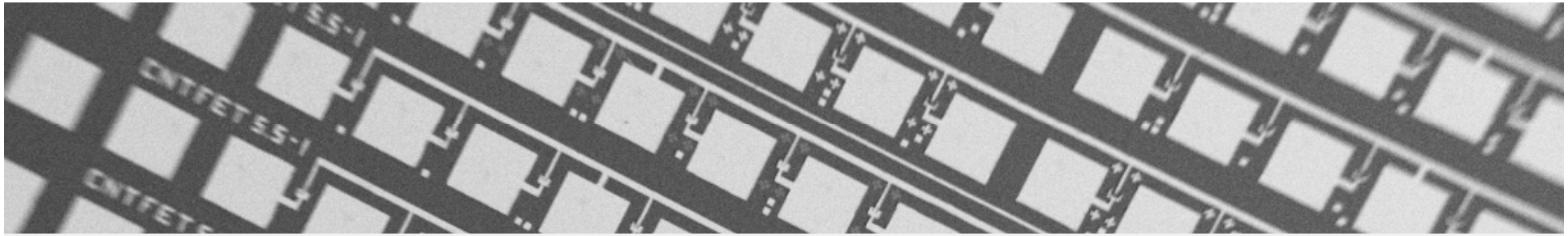
- Passivated CNT-FET based sensors* and SWCNT based antenna systems** are being developed.



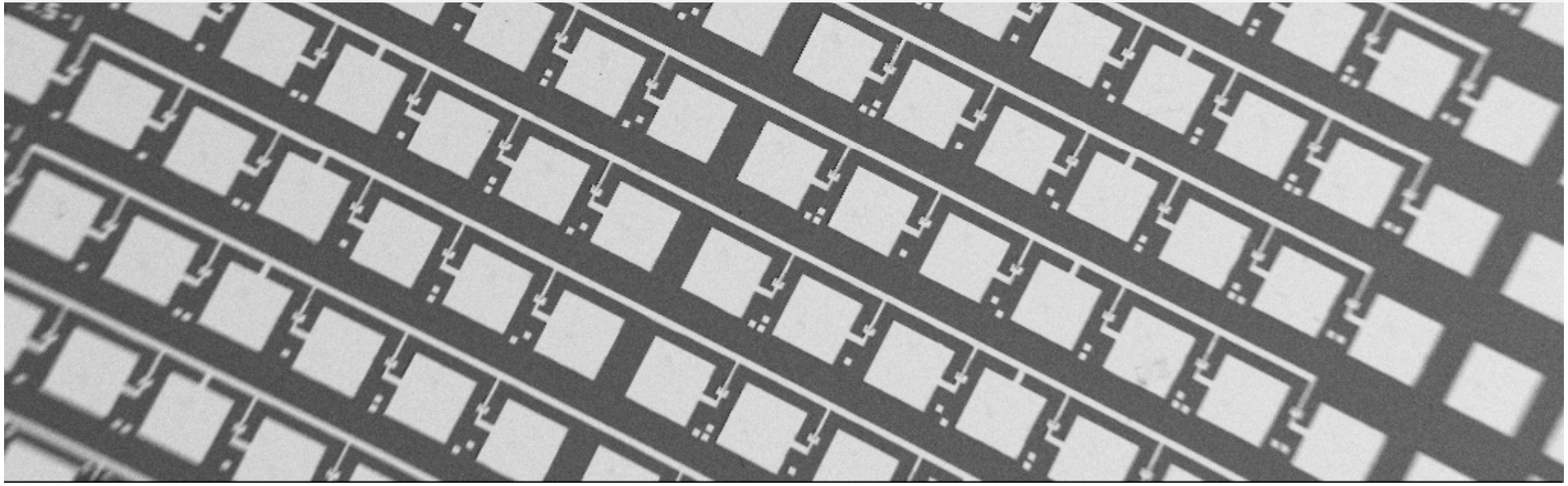
Acknowledgements

- IMB-CNM's Clean Room staff for their help with the device fabrication.
- Mr. Sergi Sanchez for support with electrical characterization.
- Dr. Narcis Mestres from ICMAB-CSIC for support with Raman measurements on CNTs.

- Financial support from CRENATUN and SENSONAT projects and from a grant through the I3P programme.



Massive fabrication of Single-Walled Carbon Nanotube Field Effect Transistors



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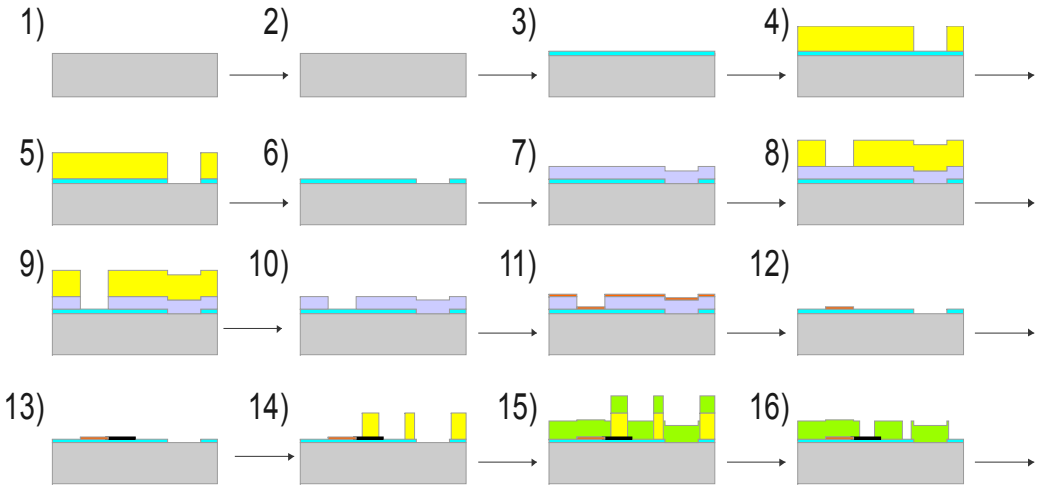
Technological process



1. 4 inch Si wafer
2. P doping of the wafer
3. Thermal oxidation: 100 nm
4. Photolithography
5. Dry etching of the SiO_2
6. PR removal
7. PMMA deposition
8. Photolithography
9. O_2 plasma
10. PR removal
11. Catalyst deposition: $Fe(NO_3)_3 \cdot 9H_2O/Mo/Al_2O_3$ in methanol
12. Catalyst lift-off
13. CVD synthesis: 800ºC, H_2, CH_4/H_2
14. Photolithography
15. Metal deposition: Ti/Pt
16. Metal lift-off

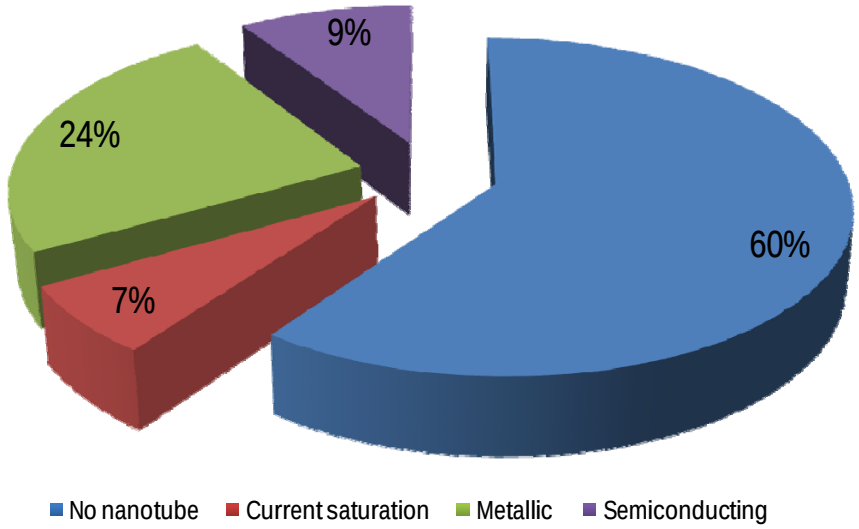
Carbon nanotube growth system

100ST Rapid Thermal CVD (Jipelec)

- ❑Temperature up to 1200 ºC
- ❑ Temperature control up to 30 ºC/s
- ❑ Controlable vacuum: 10^{-1} Torr
- ❑ Max. Vacuum: 10^{-6} Torr
- ❑ Gases: CH_4, H_2, N_2O, N_2, Ar
- ❑ Up to 4” wafers

Global results

Device type distribution for on a 4” wafer:*

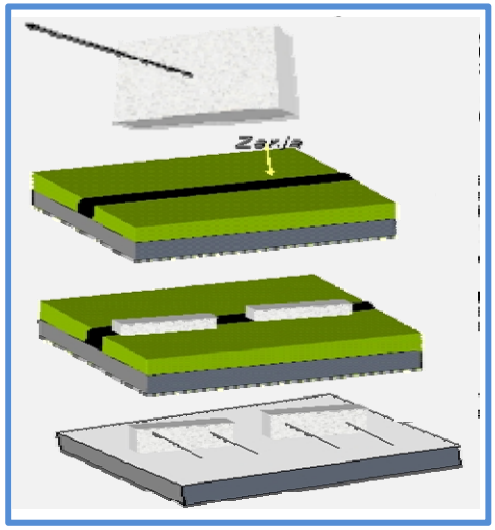


- Up to 98 functional CNT-FET ($4x4\mu m^2$ & 5µm and $5x5\mu m^2$ & 7µm)
- 10,135 functional CNT-FET on a 4” wafer (7.3 % of the total*)

  * 9.2 % of the total if 1µm gap designs are discarded
- $\frac{\text{Semiconducting}}{\text{Metallic}} = 1/2 \quad [\neq 2]$

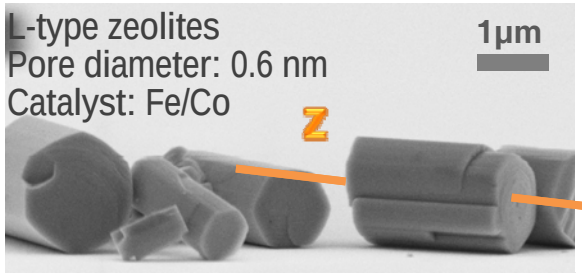
Synthesis of SWCNTs from Fe particles using zeolites*

Zeolites: Microporous materials with oriented pores of less than 1 nm in diameter.

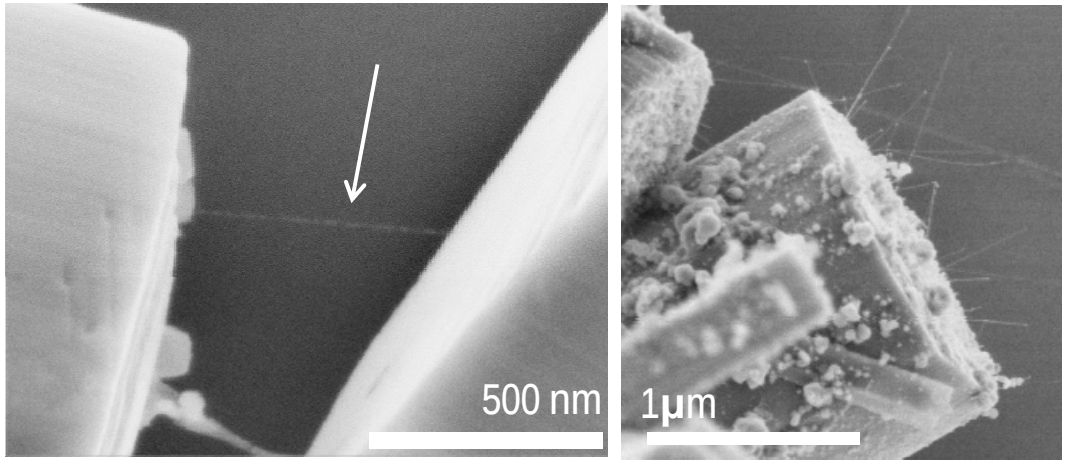


By placing catalyst inside the pores:

- ❑ Certain control over CNT diameter
- ❑ Control over CNT growth direction



☺ **SWCNT growth from inside zeolites pores**



I. Martin, et al., Microelectronic Engineering 85, 1202-1205 (2008)

*** In collaboration with Insto. Tecnología Química (ITQ-CSIC)**