FABRICATION OF HfO_2 PATTERNS BY NANOSCALE LITHOGRAPHY METHODS AND SELECTIVE DRY ETCHING FOR III-V CMOS APPLICATION

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The replacement of silicon channels by high carrier mobility III-V semiconductors, i.e. GaAs, InGaAs, in combination with Hf-based high-k gate dielectrics offers the possibility of reduced power consumption and enhanced performance for metal-oxide-semiconductor field-effect transistors (MOSFET) in future technologies.[1] Both conventional single-gate and novel multi-gate device architectures based on high-k/III-V stacks [2,3] will need the development of fabrication processes that meet the stringent requirements of the ITRS roadmap. Of particular importance is the availability of a reliable process for the selective etching of ultra-thin HfO_2 layers on GaAs. Key requirements are a high degree of reproducibility in terms of etch rate control, HfO_2 etch selectivity, i.e. the ratio of the HfO_2 etch rate to the GaAs etch rate, high anisotropy, absence of GaAs lattice damage, and potential application to gate stack nanopatterning.

Dry etching of HfO_2 films deposited on silicon substrates has been extensively studied using several plasma chemistries based on fluorine (F), chlorine (Cl), bromine (Br), and methane (CH_4).[4-9] By contrast, no studies have been reported to date relative to nanopatterning and etching of HfO_2 layers deposited on GaAs substrates. In this work, we investigate the reactive ion etching (RIE) characteristics of ultra-thin HfO_2 layers (10-15nm) deposited on GaAs, using two plasma chemistries, BCl_3/O_2 and SF_6/Ar, with specific emphasis placed on the optimization of the etch selectivity, etch depth control and surface morphology of the underlying GaAs substrate. Our study shows that etching in a BCl_3/O_2 plasma leads to a poor selectivity of HfO_2 over GaAs due to the relatively fast etching rate of GaAs in this ambient. But the lower volatility of the reaction products between GaAs and F slows down the GaAs etch rate in the SF_6/Ar plasma, which combined with the sputtering action of Ar allows for an adequate control of the HfO_2 etching rate and good etch selectivity (1.5) with respect to the GaAs substrate.

Two lithographic techniques, namely e-beam (EBL) and laser interference nanolithography were used to fabricate of deep-submicron HfO_2/GaAs structures. After masking the HfO_2/GaAs samples with polymethylmethacrylate (PMMA) resist, different patterns consisting of open stripes with nominal widths between 100 and 500 nm were transferred by lithography. Subsequently, the exposed HfO_2 areas were selectively removed by RIE in a SF_6/Ar plasma. Morphological and compositional characterization of the resulting nanopatterns by atomic force microscopy (AFM), high-resolution scanning electron microscopy (HRSEM), energy-dispersive X-ray spectroscopy microanalysis (EDX), and transmission electron microscopy (TEM), has shown the formation of well defined HfO_2 structures with nanometre-scale line width control and anisotropic profiles. In addition, atomically smooth, stoichiometric and residue-free bottom GaAs etched lines with a lateral dimension of ~50 nm have been achieved, thus demonstrating the feasibility of SF_6/Ar plasma processing to nanopattern high-k gates in advanced CMOS fabrication.

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Figures

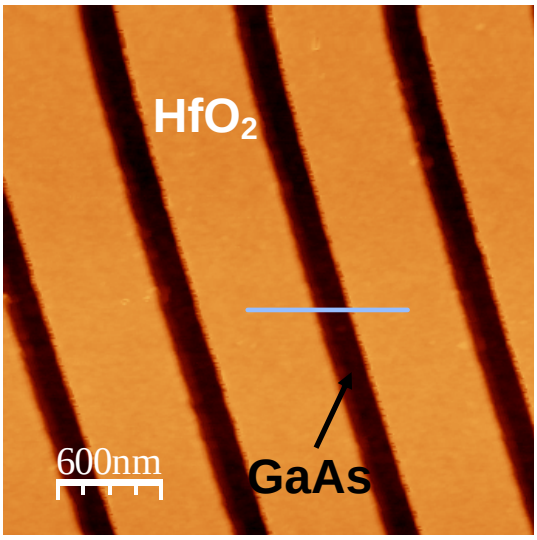

Figure 1. AFM image (3μmx3μm) of the patterned HfO_2 surface morphology showing a series of 200nm-wide etched trenches

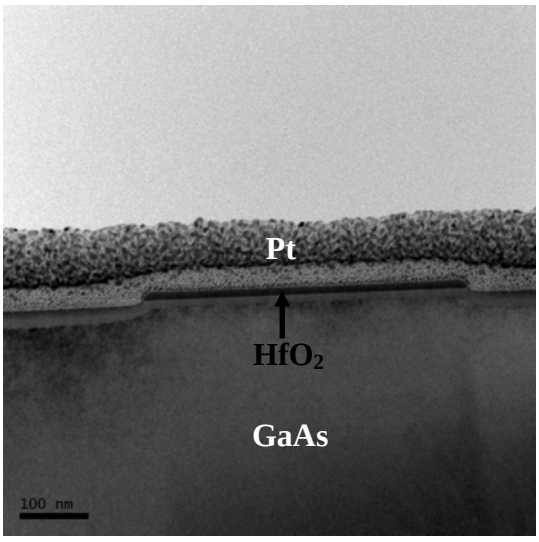

Figure 2. TEM cross section images of a 400 nm-wide HfO_2 mesa stripe after etching in SF_6/Ar plasma.