Design of 6T SRAM memory cell using a SB-CNTFET compact model

M. Najari[1,2], S.Frégonèse[1], C. Maneux[1], T. Zimmer[1], H. Mnif[2], N. Masmoudi[2]

[1] Université de BORDEAUX, CNRS, UMR 5218, FRANCE,
[2] National School of Engineering of Sfax – LETI Laboratory - Sfax, TUNISIA,
montassar.najari@ims-bordeaux.fr

This work presents a compact model formulation for the Schottky barrier carbon nanotube field effect transistor (SB-CNTFET). Compact model as well as Monte-Carlo I-V simulated characteristics will be compared to each other and also to experimental data in order to validate the used approximations. Then, for the assessment of the Schottky barrier on circuit performances, traditional 6T SRAM memory cell is designed using the SB-CNTFET compact model. Transient power consumption results are compared with those of the conventional CNTFET with zero-SB height.

The SB-CNTFET (Fig. 1) used in this work is presented in detail in [1]. In this model, for calculating the SB height, an approximation method based on recent works from [2] is adopted. This approximation consists in solving analytically the 1D modified Poisson equation for the channel potential and so calculating an effective SB height (Fig. 2). This effective SB height (Fig. 2) is expressed as [2]:

$$\phi_{SB\_S,D}^{eff} = \left(\phi_{SB\_S,D} - qV_{S,D}\right) e^{\left(-d_{tunnel}/\lambda_{Schottky}\right)} + qV_{S,D} \quad (1)$$

, where d_{Tunnel} is the tunnelling distance which scales as $1/\sqrt{m^*}$ [3]. $\lambda_{Schottky}$ is the screening length related to d_{Tunnel} as well as t_{ox} (oxide thickness) [1]. The screening length reflects the device geometry [4].
Hence, the linear charge density n_{CNT} in the SB-CNTFET is derived analytically from piece-wise calculation of the Fermi distribution and of the density of state relative variation [5].

In the other hand, the drain current is calculated by means of the Landauer–Buttiker formula [6] assuming a one dimensional ballistic channel in between the SBs [5]:

$$I = \frac{4ek_BT}{h}\sum_{p=1}^{+\infty}\left[\ln\left(1+\exp\frac{eV_S + \Phi_{SB\_S}^{eff} - sbbd\left[p\right]}{k_BT}\right) - \ln\left(1+\exp\frac{eV_D + \Phi_{SB\_D}^{eff} - sbbd\left[p\right]}{k_BT}\right)\right] \quad (2)$$

A comparison between the SB-CNTFET compact model I-V results and the Monte-Carlo simulations of transistors [7] for a wide range of gate to source and drain to source voltages has been performed (Fig. 3). A good agreement is found between compact model results and Monte-Carlo simulation for both I_D vs. V_{GS} and I_D vs. V_{DS} excepting at high V_{DS} values .This is mainly due to effects of optical phonon (OP) scattering and radial breathing mode (RBM) scattering which are not taken into account in the current version of the compact model. Future works will tackle these limitations.

Measured I_D vs. V_{GS} characteristic of an SB-CNTFET with back gate configuration has been presented in [8]. Compact model results are compared to these measured curves (Fig. 4) and good agreement is observed over a large range of gate to source V_{GS} voltage (from -2V to 2V) and drain to source V_{DS} voltage (from -0.1V to -0.7V).

A traditional 6T SRAM memory cell [9] is designed using the SB-CNTFET compact model. Fig. 5 shows the simulations results of the read and write waveforms for a 6T-SRAM memory cell at 0.5V of power supply voltage. On this figure, the cell exhibits the desired memory effects either for low "0" and high "1" logical levels. To point out the effect of the SB on cell dynamic's performances; the power consumption for the SB-CNTFET based 6T SRAM cell is compared with the MOS-like CNTFET.

Fig. 6 shows the transient power consumption curves for the write and read operations of "0" and "1" logical level related to the MOS-like CNTFET and the SB-CNTFET. These curves prove that SB-CNTFET consumes less than the MOS-like CNTFET for either read and write operations. However, its power-delay product is higher than the MOS-like CNTFET.

This paper proposes an efficient compact model for the SB-CNTFET. The proposed model has been verified against Monte-Carlo simulations and measured data. The results are shown to match very well over a large range of biases. Hence, it argues the validity of the used approximations. Since the developed compact model is suitable for circuit simulation in Spice like environment, 6T SRAM static memory cell is designed in EDA tool. The impact of the SB on such applications performances is pointed out by showing the transient power consumption curves in comparison with the MOS-like CNTFET at zero SB height.

Figures

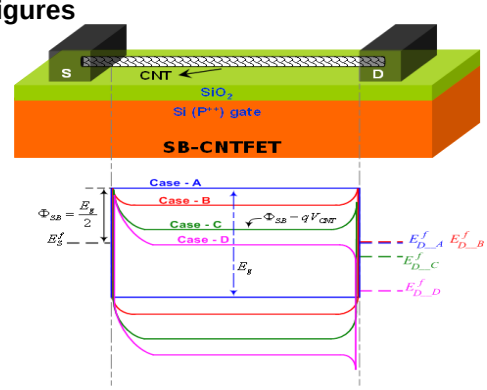

Figure 1. (up) Artistic view of a SB-CNTFET and corresponding energy band diagram **(down)** at various V_{GS} and V_{DS};(Case-A: V_{GS}=V_{DS}=0, Case-B: V_{GS}>0 V_{DS}=0, Case-C: V_{GS}>V_{DS}>0 and Case-D: V_{DS}>V_{GS}>0).

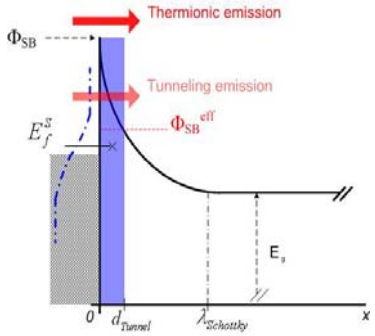

Figure 2. Effective Schottky barrier approximation. The tunneling probability through the SB is set to unity if the barrier at some energy is thinner than d_{Tunnel} and zero otherwise.

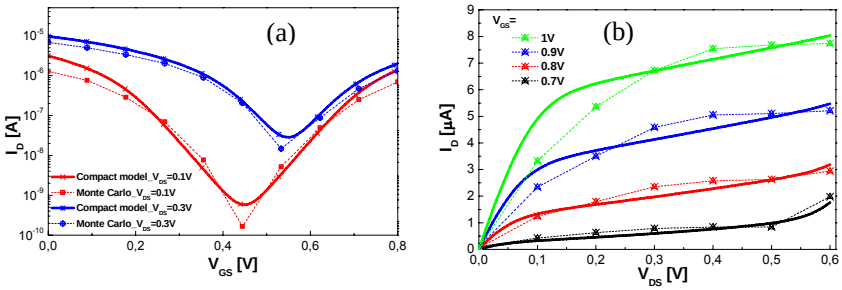

Figure 3. (a) Simulated I_D-V_{GS} characteristics from the compact model (solid lines) and Monte-Carlo (dashed symbol lines) of a Schottky barrier CNFETs adopted from [7] for a channel length of 100nm and an oxide thickness t_{ox} equal to 5.3nm. The S/D Schottky barrier height is Φ_{SB}=0.275eV.
(b) I_D-V_{DS} characteristics for different values of V_{GS} and for a Schottky barrier height Φ_{SB}=0.275meV, L =100nm and t_{ox}= 5.3nm.

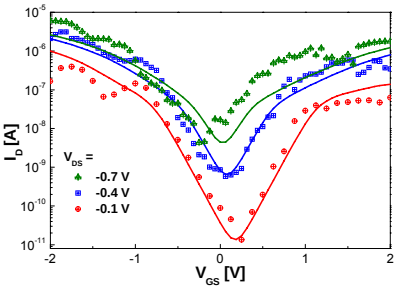

Figure 4. I_D vs. V_{GS} simulated (lines) and measured (symbols) characteristics [8] for a SB-CNTFET with (14, 0) CNT for three V_{DS}, -0.1V, -0.4 and -0.7V. t_{ox}=10nm of SiO_2 and Ti made contacts → Φ_{SB}=110meV.

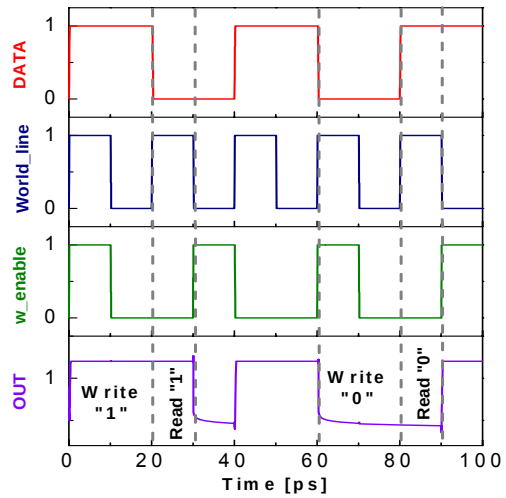

Figure 5. Simulated waveforms of the read and write operations for a 6T-SRAM cell designed with the SB-CNTFETs, Φ_{SB}=0.2eV.

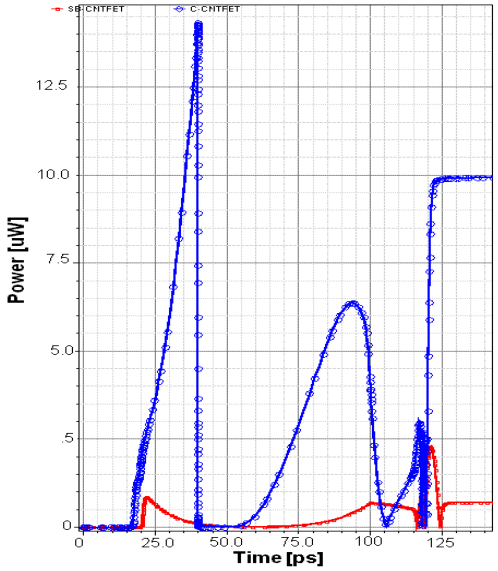

Figure 6. Transient power consumption of writing operation of "0" (a) and "1" logical level for the CNTFET and the SB-CNTFET, Φ_{SB}=0.2eV @ V_{DD}=0.5V.

References

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