Non-volatile memory using Optically-Gated Carbon Nanotube FET: Description of carrier mobility model in P3OT and hopping mechanism at SiO_2-P3OT interface

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The operation of Optically-Gated CNT field effect transistor (OG-CNTFET) has been demonstrated by using photo-generated electrons density to modulate the channel potential as well as the electric gate [1]. This device (Fig. 1) which presents non-volatile memory property is particularly interesting for neuromorphic network design to build the learning circuit [2]. To answer the requirement of CAD simulation, a compact model is developed to describe the OG-CNTFET operation using a physical and behavioral mixed approach [3]. Recently, Schottky metal-CNT contacts have then been taken into account in this model because of the importance of the remarkable barrier height at source and drain contacts [4]. In this paper, the physical meaning of the model is further enhanced. Since the relaxation recombination mechanism of the photo-charged OG-CNTFET is modeled by the P3OT conductivity expression while in [3, 4], it was modeled through an empirical current source. By developing the P3OT conductivity expression, we provide a detailed physical based model of the OG-CNTFET which more accurately describes the carrier relaxation mechanism.

Photo-generated electrons are held in deep traps at the SiO_2-P3OT interface when the electric gate bias is null. We assume that the relaxation of OG-CNTFET is associated with the electron hopping mechanism from deep traps to the CNT channel. To model the relaxation, we calculate the intrinsic conductance between interface traps and the channel. Two general methods have been reported to describe the carrier mobility of P3OT and P3HT which are widely used in solar cells: Pool-Frenkel model (PF) and Gaussian disorder model (GDM) [5]. We integrate PF mobility (μ_{P3OT}) into the expression of P3OT conductivity (σ_{P3OT}) thanks to the good fitting in the low electric field range [5] corresponding to the non-volatile memory operation condition.

$$\mu_{P3OT} \approx \mu_0 \exp\left(-\frac{E_0}{kT}\cdot\frac{T_R - T}{T_R}\right) \Rightarrow \sigma_{P3OT} \approx N_{trap} e \mu_0 \exp\left(-\frac{E_0}{kT}\cdot\frac{T_R - T}{T_R}\right)$$

The expression of mobility is simplified from ref [5]. The field dependence in the exponential is negligible because the channel potential supposes to be uniform to present a ballistic transport in our compact model. Therefore, in the P3OT layer, the electric field doesn't take place as well as in the CNT channel. E_0 is the activation energy of interface traps without electric field. T_R is the empirical reference temperature for associated known P3OT mobility. N_{trap} represents the density of occupied traps. We use optimized values from ref. 5: E_0 is equal to 0.165 eV; T_R is equal to 700 K; μ_0 is equal to 2.7 x 10^{-3} $cm^2/(V.s)$.

The recombination of trapped electron supposes that a tiny part of trapped electrons can be released thanks to hopping mechanism at the SiO_2-P3OT interface and finally evacuates through the nanotube [4]. We simplify this mechanism by a relaxation probability $Rate_{relax}$, which depends only on the temperature. Hence, the relaxation current results from the product of the voltage bias $V_{Laseri,CNT}$ times P3OT conductor Y_{P3OT} times $Rate_{relax}$.

$$I_{relax} = V_{Laseri,CNT} \cdot Y_{P3OT} \cdot Rate_{relax} = V_{Laseri,CNT} \cdot \sigma_{P3OT} \frac{area}{length} \cdot Rate_{relax}$$

$$with N_{trap} \cdot e = Q_{trap} = V_{Laseri,CNT} C_{Optic1}$$

$$\Rightarrow I_{relax} = V_{Laseri,CNT}{}^2 C_{Optic1} \cdot \mu_0 \exp\left(-\frac{E_0}{kT}\frac{T_R - T}{T_R}\right)\frac{L_G d_{CNT}}{w_{eff}} \cdot Rate_{relax}$$

C_{optic1} represents the trap capacitance [3]; L_G, d_{CNT}, and w_{eff} are device geometries [4].

In fig. 2, we compare chronograms of simulation results to experimental measurements of OG-CNTFET non-volatile memory operation [2]. The programming [3] and the gate-protected [4] programming mechanisms have been reported. The two chronograms in the first line present V_{DS} memory programming commands. The programming voltage is 4 V in the simulation, 5.5 V in measurements. The memory reading voltage is -0.4 V in both case. In the middle line, V_{DS} programs successively the photo-charged OG-CNTFET from the high to low conductivity state without the gate protection (V_G=0V). In the third line, the V_{DS} programming is stopped by a gate positive pulse of 6 V, and the devices keep their high conductivity state. Here, we focus on the states from a programming pulse to another: the drain current levels I_D are almost unchanged; i.e. they keep the last programmed state. In simulated

chronograms, the slight decrease of I_D represents the SiO_2-P3OT interface traps relaxation. The simulated device behavior is very close to the experience, but the I_{on}-I_{off} level is remarkable different. Because the measurements were achieved on a nanotube network-based OG-CNTFET [2], the I_{on}-I_{off} ratio was lower than the device with the single CNT channel [1].

References

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Figures

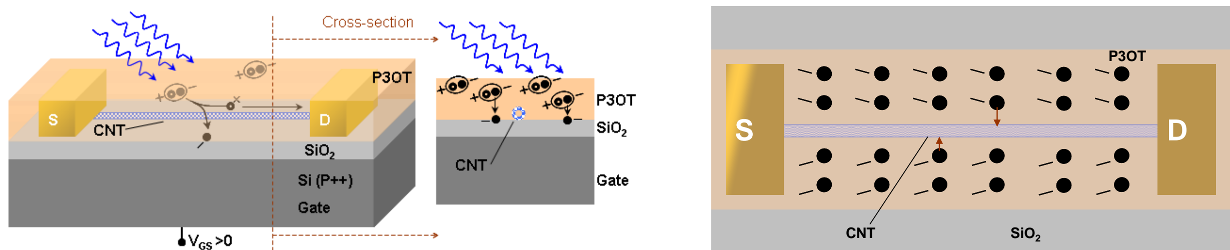

Figure 1 – OG-CNTFET description
Left, the OG-CNTFET structure scheme with the optical gating mechanism;
Right, the device relaxation resulted by the electron hopping mechanism.

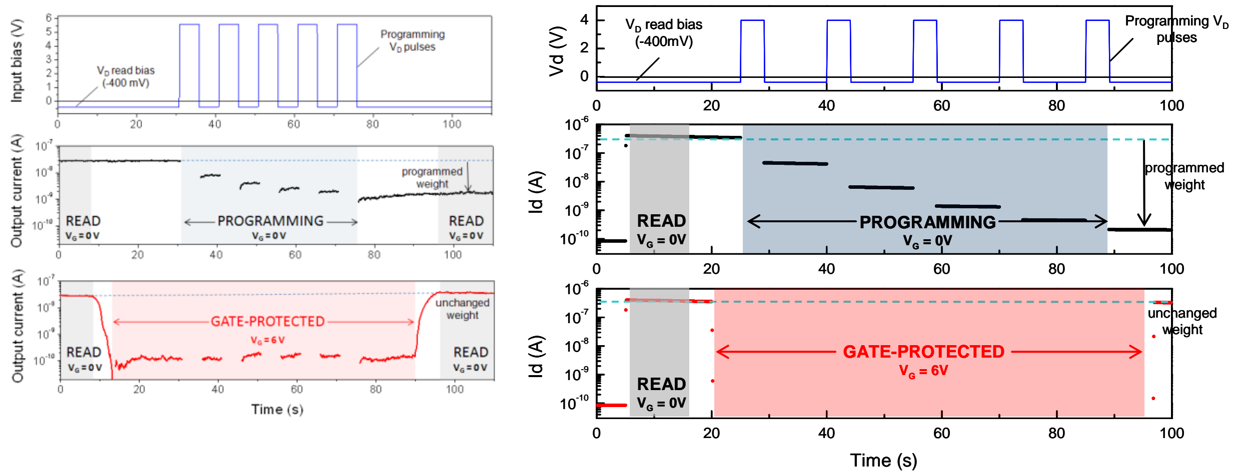

Figure 2 – OG-CNTFET operation: Chronograms of the non-volatile memory programming.
Left, the experimental measurement data with and without gate protection [5];
Right, the associated simulation results.
The programmed weight in the simulation is greater than the one in the experience since the programming in the simulation is more efficient.