A Compact Model for the Magnetic Tunnel Junction Switched by Thermally Assisted Spin Transfer Torque (STT+TAS)

Julien Duval[1, 2], Weisheng Zhao[1, 2], Jacques-Olivier Klein[2, 1] and Claude Chappert[1, 2]

1. IEF, CNRS, UMR8622, Orsay, France-91405
2. Univ. Paris-Sud 11, Orsay, France-91405
weisheng.zhao@u-psud.fr

Thanks to its non-volatility, high write/read speed and easy integration with CMOS process, Magnetic Tunnel Junctions (MTJ) has become a cornerstone of spin electronics such as the Magnetic RAM (MRAM) [1] and Magnetic logic [2-3]. The current research in MTJ nanopillar focus on the high performance (power efficient, high speed and high reliability) switching approaches, as the two high currents used in the conventional methods limit the power and die area of MTJ based circuits. Thermally Assisted Switching [4] was proposed to improve the data stability and reduce the power dissipation but it cannot overcome the miniaturization limits (~65nm). Spin Transfer Toque [5] is one of the most potential approaches to overcome these limits, as there requires only one low current for the switching. However, STT brings new problem: the degradation of thermal stability. Recently, a new approach: Thermally Assisted Spin Transfer Torque (STT+TAS) combining the advantages of both two technologies has been proposed [6], which promises low power, high density and high data stability.

The MTJ stack in Fig 1.a is slightly modified to be adapted to the TAS operation: the storage layer is coupled with an anti-ferromagnetic (AF2) layer with low blocking temperature (T_{b2} =~150°, T_{b1}=~300°) [7]. Contrary to the STT-MTJ, the storage stability is no longer based on the shape anisotropy but on the exchange bias [8], the shape of the STT+TAS MTJ is thus circular as we can see in Fig 1.b. Therefore, this stability does not depend on the volume of the MTJ which is very interesting in order to improve the scalability of the MTJ. For the writing process, a low current I_{switch} passes through the MTJ and heats the stack. When the MTJ is heated at a temperature above the blocking temperature T_{b2}, the exchange bias effect disappears and the same low current I_{switch} can switch the magnetization of storage layer. By changing the current direction of $I_{switch,}$ shown in Fig.1c and d, the state of MTJ can be switched from P (low resistance, logic ‘0’) to AP (high resistance, logic ‘1’) and from AP to P. After the switching, the temperature of MTJ is reduced below T_{b2} and the exchange bias effect reappears for the storage layer but with new magnetization direction. In order to prevent any switching of the reference layer, the blocking temperature T_{b1} of the AF1 layer should be much higher than T_{b2}. In order to develop the MTJ based memory and logic circuits, a compact model compatible with the standard IC CAD tools is necessary. Based on our previous STT-MTJ model [9], this new compact model integrates the thermal variations activated by the current or voltage pulses, temperature dependence of the MTJ switching threshold and duration [10].

In our model, a RC circuit shown in Fig.2 has been implemented in parallel with the MTJ to present the temperature evaluation. By using a multiplier (M_0) and an adder (A_0), the temperature T can be observed by the V_{temp} voltage. This TAS+STT compact model has been developed in Verilog-A language and implemented on Cadence Virtuoso platform [11]. A number of experimental parameters are integrated in this model to improve the simulation accuracy. To demonstrate the expected behaviors of STT+TAS switching approach transient simulations have been done. Fig.3 shows the simulation results of the heating and switching operations of the compact model. Only one low current I_{switch} is used for the heating and switching of MTJ (a=b=65nm, TMR=120%). The heating period for the MTJ in P to AP state is about 6.3ns and can be reduced by increasing the switching current value. As the temperature T of MTJ reaches to the blocking temperature $T_{b2,}$ the model will compare the I_{switch} with the critical switching current. In the simulation shown in Fig.3, I_{switch} is superior to the critical current I_{C0} and the switching can be done in about 5ns thanks to the spin dynamic behaviors [12].

We presented the compact model for STT+TAS switching approach based MTJ, which integrates the heating/cooling phenomena and STT dynamic switching behaviours. The model is compatible to the standard CAD tools and can be simulated directly with the CMOS design kit. The simulations and calculation of hybrid MTJ/CMOS circuit based on this model are under investigation in our laboratory.

References

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Figures

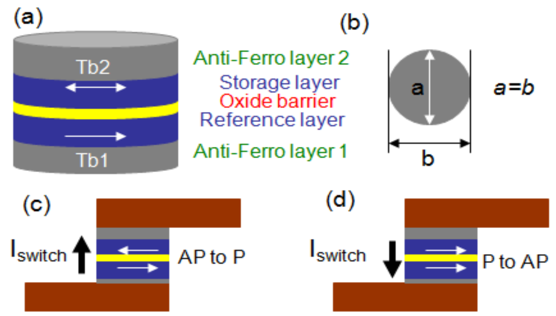

Figure 1. (a) STT+TAS switching approach: MTJ is composed of 5 layers (two anti-ferromagnetic layers, two ferromagnetic layers and one oxide barrier). (b) The shape of STT+TAS MTJ is circular. (c) and (d) The current I_{switch} passing through the STT+TAS MTJ heats it up to the blocking temperature (Tb2) and then, the same current changes the magnetization of the storage layer and programs the state of the STT+TAS MTJ.

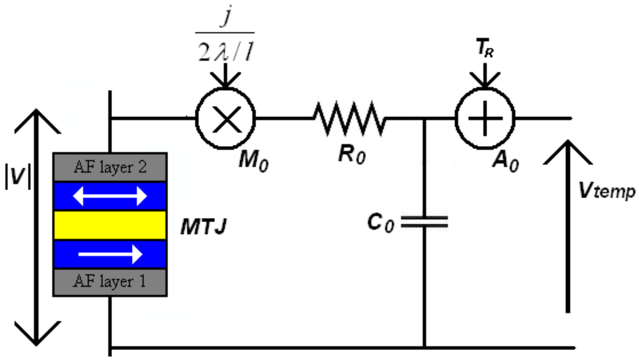

Figure 2 Electrical equivalent circuit to implement the temperature on the model.

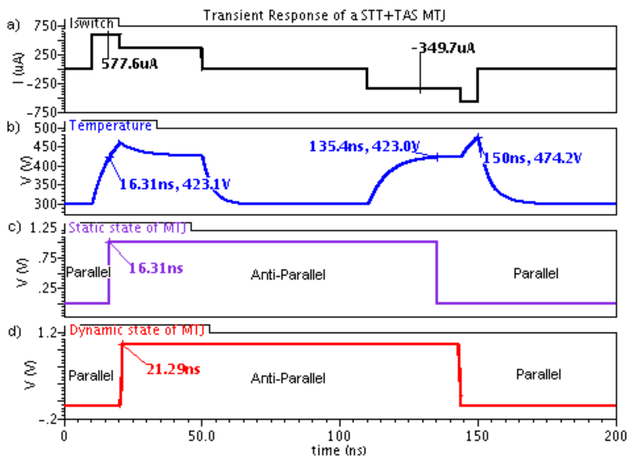

Figure 3. Transient simulation of the STT+TAS MTJ compact model. (a) The heating-switching current (400mv voltage pulse duration: 40ns and period: 100ns), the I_{switch} value is as low as 577.6uA for both heating and switching the MTJ from P to AP state in about 11ns. In order to switch the MTJ from AP to P state, the current direction is negative and the current value is about 349.7uA. (b) The temperature the MTJ increases with the current pulse. The MTJ in P state can be heated more rapidly than the MTJ in AP state thanks to the higher current. (c) The static switching of STT+TAS MTJ, the switch can be done as the temperature of MTJ reaches up to the blocking temperature. (d) The dynamic switching of STT+TAS MTJ, taking into account the spin dynamic behaviors [9].