Ferroelectric-gate Field Effect Transistors Based Nonvolatile Memory Devices Using p-type Si Nanowire Conducting Channel

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Ferroelectric-gate field effect transistor (FEFET) based memory using a nanowire as a conducting channel has many desirable features including small cell size, low-voltage operation, low power consumption, fast programming/erase speed and non-volatility [1]. We successfully fabricated a ferroelectric nonvolatile memory device using a p-type Si nanowire coated with organic ferroelectric PVDF via a low temperature fabrication processing technique [2,3]. The device performance was carefully characterized in terms of their electrical transport, retention and endurance time. [3]. Our FEFET memory devices exhibit excellent memory characteristics with a large modulation in channel conductance between ON and OFF states exceeding 10^5; long retention time of over $5x10^4$ s and high endurance of over 10^5 cycles while maintaining ON/OFF ratio over 10^3 (See Fig. 1, 2 and 3). This result offers a viable way to fabricate a high performance high-density nonvolatile memory device using a low temperature fabrication processing technique, which makes it suitable for future flexible electronics.

References

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[3] Hiroshi Ishiwara “Current status of ferroelectric-gate Si transistors and challenge to ferroelectric-gate CNT transistors” Current Applied Physics, 9:S2-S6, 2009.

Figures

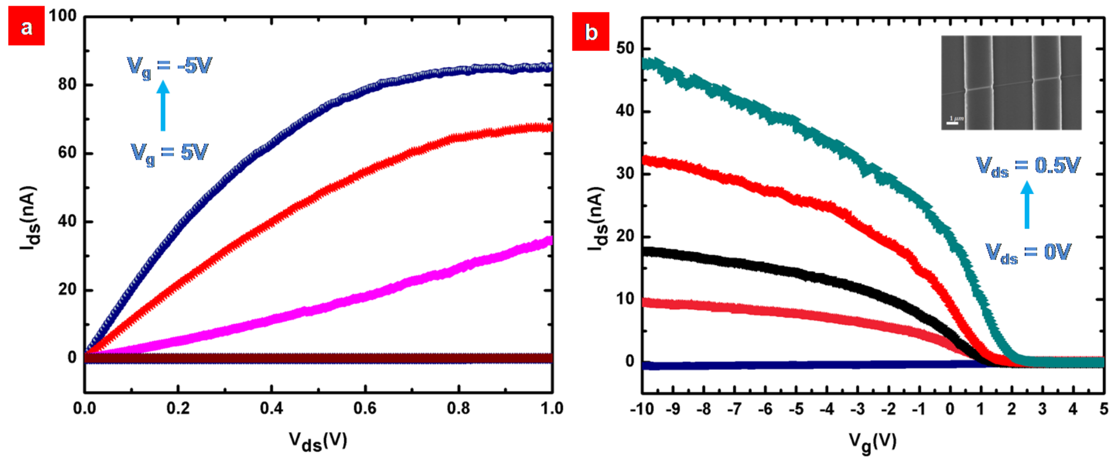

Fig.1. Electric transport properties of single Si NW FET device under ambient condition. (a) I_{ds}-V_{ds} output characteristics and (b) I_{ds}-V_g transfer characteristics at V_{ds} = 0.1 V.

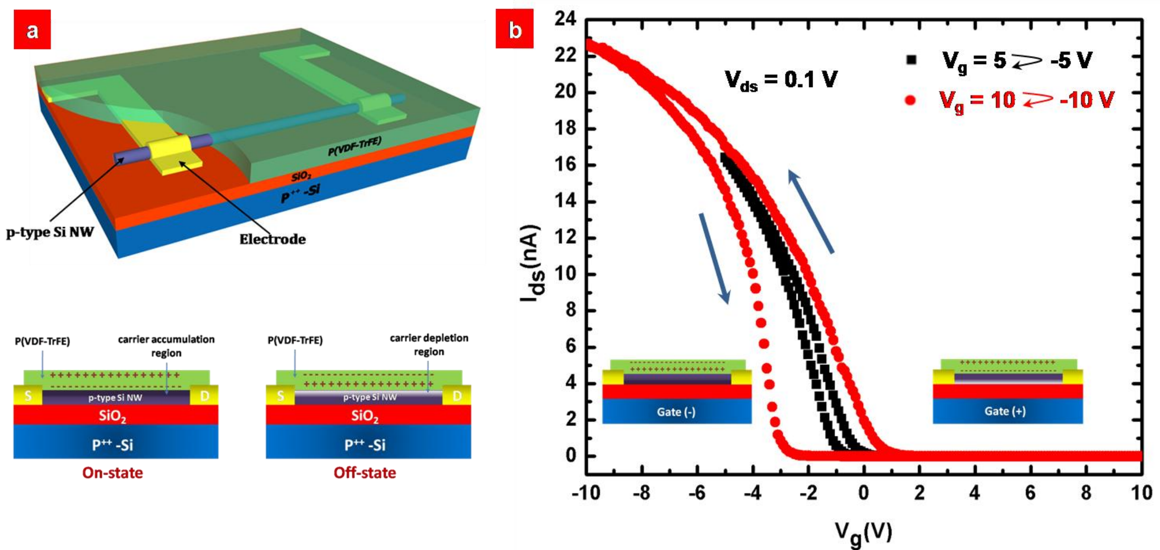

Fig.2. Si NW FFFET memory device. (a) A schematic view of a back gate FEFET based nonvolatile memory device and operation mechanism. (b) A hysteretic behavior for a back gate Si NW FEFET coated with PVDF on the NW surface.

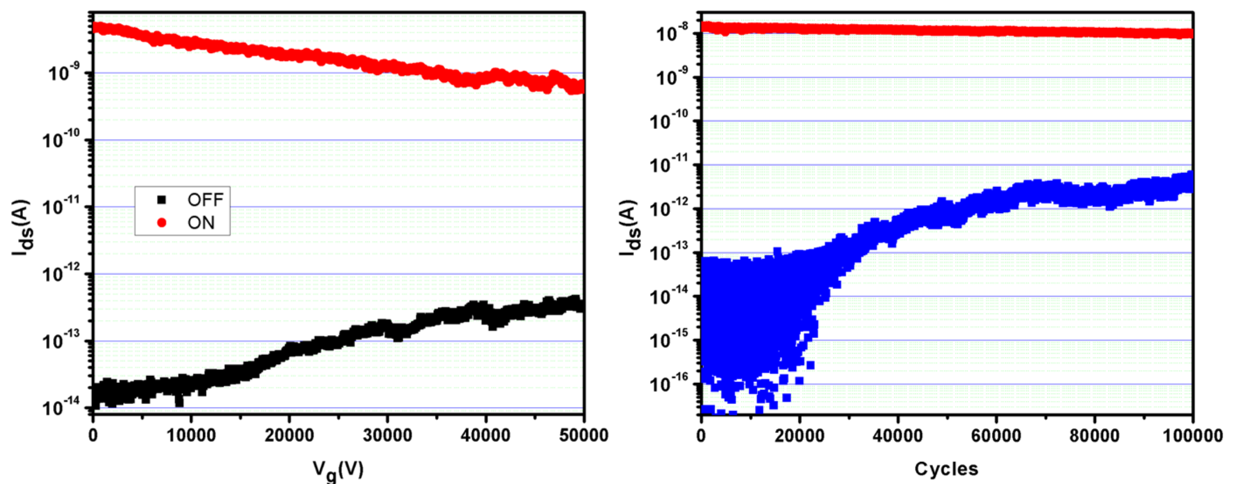

Fig.3. Memory characteristics of a Si NW FEFET (coated with PVDF) based memory. (a) Retention times and (b) Endurance tests evolution of the drain currents of the Si NW FEFET device.