Parallel Arrays of Silicon-Nanowire Field Effect Transistors for Nanoelectronics and Biosensors

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Silicon nanowires have great potential in the fields of bio chemical sensing and nanoelectronics due to their high sensitivity. However, single nanowire devices suffer from low current outputs. This work focuses in transistors made of parallel nanowire arrays that combine sufficient sensitivity with adequate current levels. Intrinsic silicon nanowires, grown by catalytic chemical vapor deposition (CVD), show electronic transport characteristics determined by the contact resistance [1]. For silicon nanowires contacted to nickel, annealing leads to axial silicidation. This results in a sharp metal-semiconductor interface which gives a fixed Schottky-barrier height along the entire contact area [2]. These wires are used as Schottky-barrier field effect transistors (SB-FETs). On/off current ratios up to 10^7 are observed for these devices. However, currents of a single nanowire FET with diameter of 20 nm are limited to approximately 1 µA and are too low for a practical sensor implementation. To enhance the maximum output current and to profit from statistical averaging, parallel arrays of nanowire SB-FETs are produced. Contact printing technique is used to transfer nanowires from the growth substrate to the chip substrate with high density and pre-defined/controlled orientation [3]. Nanowires are contacted afterwards with interdigital electrode structures by lithographical means. Significant enhancement of on-currents could be reached with these parallel arrays (0,2mA at 0.5V source drain voltage). At the same time the off-currents degrade, however the on/off current ratio is 10^3. The device fabrication with few process steps has a yield close to one which makes it feasible for commercialization. Such high-current-FET systems are appropriate for sensor systems with high readout currents and large active sensor area.

References

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[2] W Weber, L Geelhaar et al., Nano Letters, 2006 Vol6 No12, 2660-2666
[3] Zhiyong Fan et al., Nano Letters, 2008 Vol8 No1, 20-25

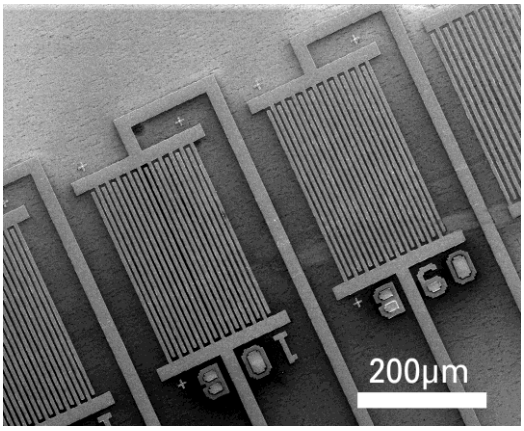

Figure 1

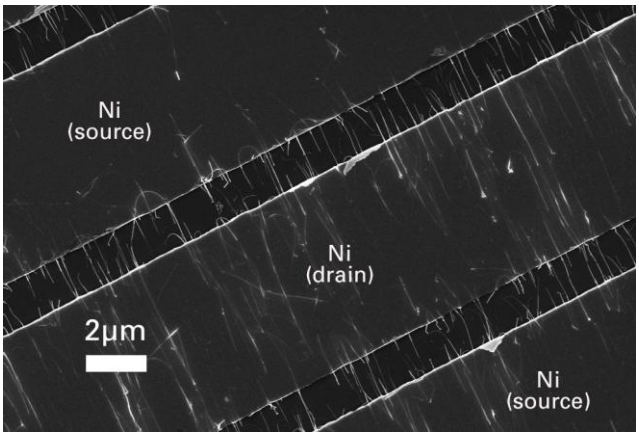

Figure 2

Figure 1: (SEM image) Interdigitated electrode structures (Ni) on 200nm thermal silicon oxide contacting silicon nanowires.
Figure 2: (SEM image) Several nanowires with intruded Nickel contacts in parallel. “Fingers” form alternating source and drain contacts. Parallel nanowire-SB-FETs are controlled via back gate.