Application of graphene to transistors: CVD growth, nanoribbon formation, and electrical properties

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Graphene, a two-dimensional honeycomb carbon lattice, has excellent electronic, thermal, and mechanical properties. It is therefore considered to be a promising material for future electronics devices. In fact, our final goal is to use graphene as a transistor channel for future large scale integrated circuits (LSIs). In order to realize it, however, there are still many issues to address. One of them is to synthesize graphene uniformly all over a large substrate. Another issue is to form a bandgap in graphene, which is essential for obtaining a high on/off ratio in graphene transistors. Optimizing the structure of a graphene transistor, which includes the choice of electrode and insulator materials, is also an important issue. Furthermore, we have to develop a good fabrication process for graphene transistors. In this presentation, we mainly address the first two issues above. First, we demonstrate graphene growth over a 200-mm wafer by chemical vapor deposition (CVD) [1, 2]. We then describe self-organizing formation of graphene nanoribbons (GNRs) on steps of a Cu surface [3]. We also explain our recent results on patterning of GNRs by Helium Ion Microscope (HeIM) and the on-off operation of a GNR transistor thus fabricated [4].

Graphene was grown on a Cu film deposited on a SiO_2/Si wafer using C_2H_4 or CH_4 diluted by Ar/H_2 as the source gas. The total gas pressure was typically kept at 1 kPa. The typical growth temperature was 860ºC. The thickness of Cu films was 500 nm or 1000 nm. The substrate was first annealed for 20 min in Ar/H2 mixture (10:1), and hydrocarbon was then added for growth. The growth time and the partial pressure of the hydrocarbon were changed to optimize the growth condition. The synthesized graphene was characterized by scanning electron microscopy (SEM), transmission electron spectroscopy (TEM), and Raman spectroscopy. Figure 1(a) shows a 200-mm Cu/SiO_2/Si wafer on which graphene was grown [1, 2]. In this case, the partial pressure of C_2H_4 was 0.59 Pa and growth time was 4 min. Raman spectra taken at 5 different positions on the wafer are shown in Fig. 1(b). The Raman spectra suggest that graphene was uniformly grown all over the wafer. Figure 1(c) shows a cross sectional TEM image taken around the center of the wafer, showing graphene formation. A bright-filed TEM image and the corresponding selected area electron diffraction (SAED) pattern are shown in Fig. 1(d) and (e), respectively. It can be seen that three sets of diffraction patterns, which are very close to each other, exist. SEM results (not shown) show that the grain size of this graphene sample is estimated at ~1 μm. Therefore, this result suggests that graphene grains are almost in the same direction. We also investigated how the size of graphene grains depended on the growth conditions and found that the size increased with decreasing the partial pressure of C_2H_4, as discussed in ref. 5. However, we also obtained results suggesting that the grain size and direction were affected by the surface morphology of Cu. Incidentally, when the total pressure was low (~100 Pa) with CH_4 as the source gas, we often observed preferential graphene growth on steps of Cu substrate, as shown in Fig. 1(f) [3]. The existence of high-index surfaces at steps is considered to be a reason for this preferential formation.

We also made GNRs by direct etching of graphene with HeIM [4]. For this purpose, single layer graphene flakes were mechanically exfoliated from HOPG using adhesive tape, and then deposited on a silicon wafer with a 300-nm-thick thermal oxide layer. On the obtained graphene flakes, source (S) and drain (D) electrodes were made by electron-beam lithography, followed by Ti/Au (5/30 nm) depositon and lift-off. A GNR with 5 nm width and 50 nm length was then patterned by irradiation of He ion beams as shown in Fig. 2(a). Here, source and drain regions are separated by the dark region where graphene was removed by He ion etching. A GNR was formed in the middle of this dark region, as highlighted by a broken circle. A schematic of the GNR device is shown in Fig. 2(b). Figure 2(c) represents the back gate bias dependence of the drain current at different drain biases at T = 45 K. The drain current is strongly suppressed between -10 V and 0 V. Most of the spike-like peaks are reproduced by multiple measurements, suggesting that these peaks reflect the resonant conduction through localizing states characteristic to each GNR. The on-off ratio at V_d = 1 mV is estimated at about two orders of magnitude. This ratio decreases as the drain bias increases, and almost disappears when V_d > 200 mV. The back gate bias range, ΔV_g, that corresponds to the transport gap, is estimated at about 10 V. From this value, the transoprt gap enrgy scale is evaluated to be ~200 meV [6]. To our knowledge, this is the first on-off operation of a GNR transisor fabricated with HeIM.

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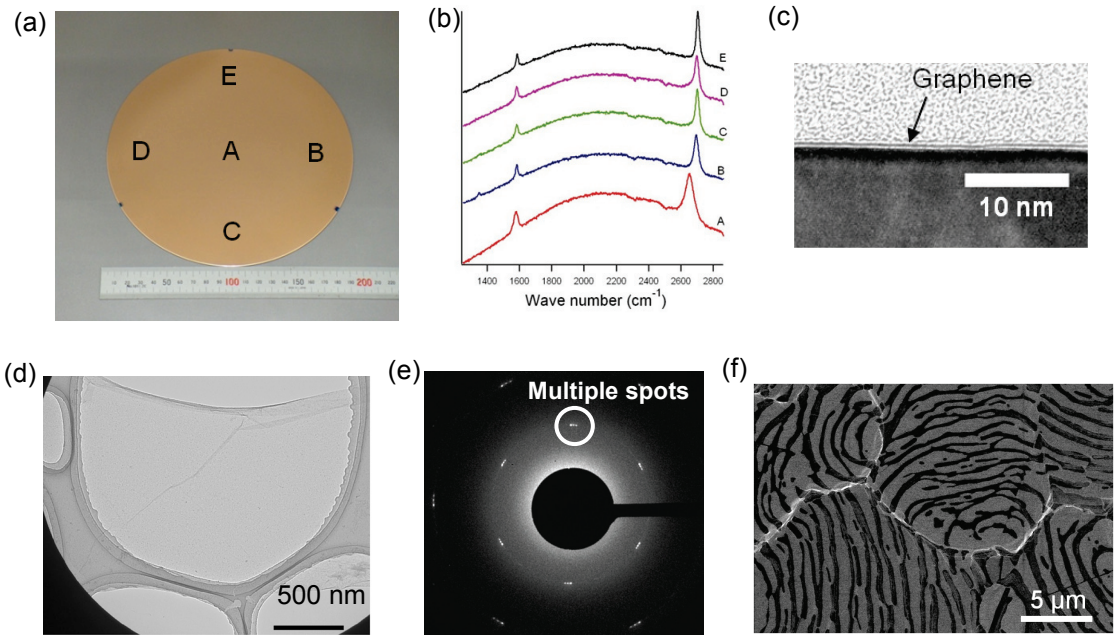

Figure 1. (a) Graphene synthesized on a Cu film deposited on a 200-mm Si/SiO_2 wafer. (b) Raman spectra of graphene at positions of A-E shown in (a). (c) A cross sectional TEM image of the graphene around the center of the wafer. (d) Bright field image of graphene on a TEM grid. (e) Selected area diffraction pattern obtained from a circular area of graphene partially shown in (a). (f) GNRs grown on steps on Cu.

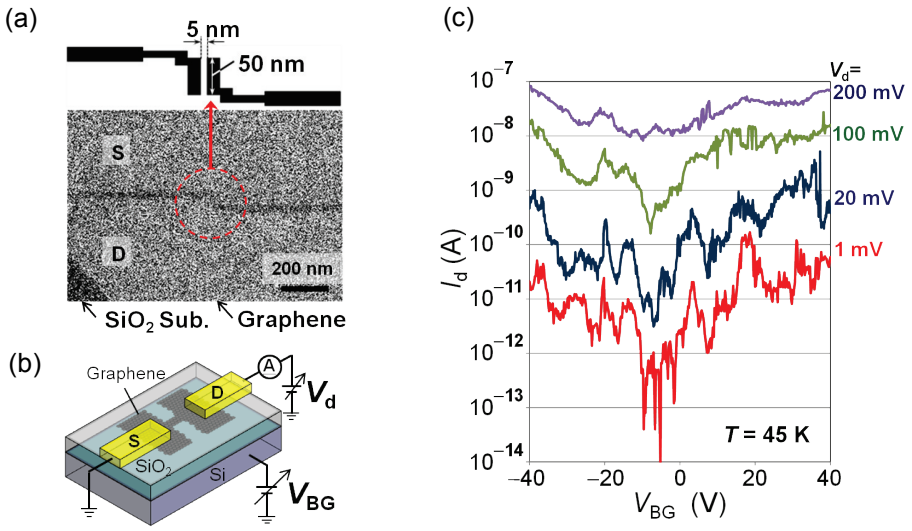

Figure 2. (a) Helium ion micrograph of a GNR with a schematic illustration. Graphene was removed in the dark region between the source (S) and drain (D). (b) A schematic of the GNR device. (c) Back gate bias (V_{BG}) dependence of drain current (I_d) at different drain biases (V_d) at T = 45 K.