A Reconfigurable Architecture Based on Spin MOSFET

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Spintronics is expected to provide wide variety of application of next generation circuit. Here we present one of promising application of spin MOSFET as Field Programmable Gate Array (FPGA) (spin FPGA). Spin MOSFET is composed of MOSFET whose source and drain are contacted with ferromagnetic materials[1]. Magnetization directions affect current through spin-torque transfer[2]. We model the spin MOSFET by describing a high resistive magnetic state with smaller mobility in SPICE parameters. SRAMs in Look-up table (LUT) and those attached to pass transistors other than multiplexers are replaced by spin MOSFET. This reduces the number of transistors and makes LUT and switching box(SB) smaller resulting in faster and smaller FPGA. Spin FPGA are benchmarked over 20 circuits by modifying VPR[3] with Monte Carlo method. Performance is improved for smaller transistors (Fig.1). For 22nm transistors, area is reduced averagely by 16% and speed (critical path delay) is improved by 24%. As MR ratio increases, operation margin increases, and as transistor size decreases, impedance of wire part increases relatively. These result in better performance of spin FPGA[4].

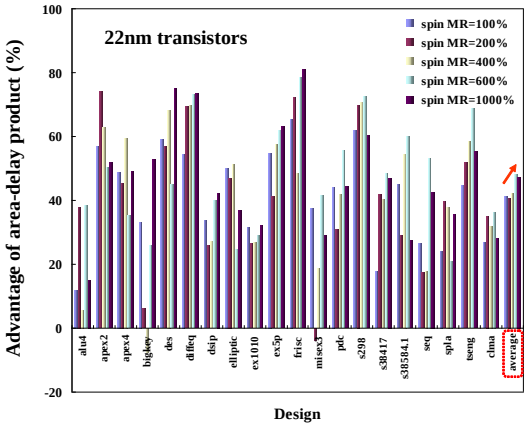

Fig.1: Benchmark calculation of the advantage of spin FPGA to CMOS FPGA over 20 circuits (area-delay product). Leftmost data shows average over the 20 circuits. As MR increases, spin FPGA shows better performance.

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[3] V. Betz, J.Rose and A. Marguardt, “Architecture and CAD for Deep-Submicron FPGAs”, Kluwer Academic Publishers, 1999.

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