## Oral senior

## CMOS compatible $\mu$ -TEG based on single crystalline Si thin films

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Thermoelectric materials permit the direct conversion of waste heat recovering useful energy as electricity. Nowadays these materials are not competitive in terms of efficiency conventional thermal machines when large amount of energy are required, but thanks to their simplicity can offer an alternative in small-scale application or when mobility is required [1]. In thermoelectric materials the efficiency in energy conversion can be described through the figure of merit ZT, defined as

$$ZT = \frac{\sigma \cdot S^2}{k} T$$

Nanostructured semiconductors offer a promising route towards the fabrication of miniature chipbased TE devices. In particular, Si has emerged as a potential TE candidate since the discovery that small diameter nanowires (NWs) conduct heat like a disordered solid  $(k\downarrow)$  [1], maintaining reasonable values for both electrical conductivity ( $\sigma$ ) and Seebeck (S) coefficient. Consequently it is expected an enhancement of the thermoelectric conversion efficiency. In this context, the fabrication of miniature chips formed by Si NWs arrays may yield efficient conversion devices. While bottom-up strategies for the synthesis of NWs allow the realization of highly-dense large-area arrays of NWs [2], they often lack enough reproducibility.

Here, we present a planar TE microgenerator based on top-down fabricated that can work up to T  $\sim$  700 K. The design is based on a free-standing membrane, that should act as a cold or heat removal sink, suspended from a bulk Si frame, acting as heat source, through silicon thin films (100nm thick) with regions doped p and n (see figure 1). This structure is achieved by using CMOS

compatible microfabrication techniques starting with a SOI wafer. To obtain the appropriate doping level we carried out detailed TRIM simulations and multiple implantation and annealing experiments. Doping levels in the range of  $1\text{-}5x10^{19}$  at/cm³ both in n and p-type regions are obtained and epitaxial re-crystallization of the 100 nm thick Si layer is reached during post-implantation thermal treatments. Suitable electrical contact resistances, i.e.  $1.5x10^{-5}~\Omega\text{cm}^2$ , were achieved by using 100nm Ni thin layers and post-deposition annealing to form NiSi.

The microgenerator is equipped with Au heater/sensors, placed in membrane and Si frame, to completely determine the thermoelectrical performance of the device (see figure 2). We do obtain an improvement of 50% in the ZT of the whole device compared with the bulk Si values. For T gradients of 200K the device generates more than 4 mW/cm<sup>2</sup>.

## **References**

- [1] Lon E. Bell, Science 321, (2008) 1457-1461.
- [2] L. Shi, D. Li, C. Yu, W. Jang, D. Kim, Z. Yao, A. Majumdar, J. of Heat Transfer 125 (2003) 881-888.
- [3] D.Davila, A.Tarancón, C.Calaza, M.Salleras, M.Fernandez-Regúleza, A.San Paulo, L.Fonseca. Nano Energy 1 (2012) 812–819.
- [4] A.P.Perez-Marín, A.F.Lopeandía, L.Abad, P.Ferrando-Villaba, G.Garcia, A.M.Lopez, F.X.Muñoz-Pascual, J. Rodríguez-Viejo, Nano Energy, 4 (2014) 73-80.

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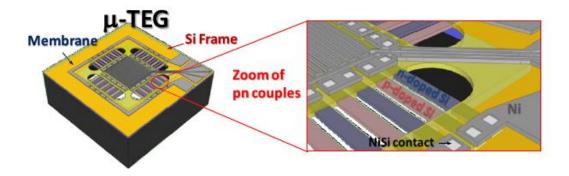
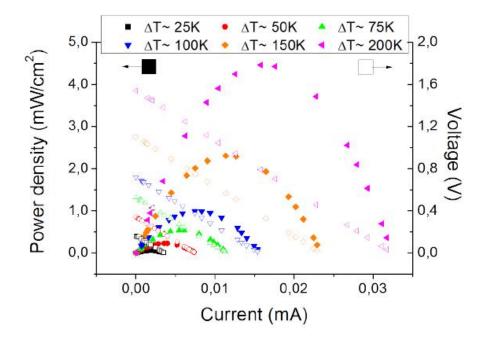


Figure 1. Schematic of the m-TEG.



**Figure 2.** Thermoelectric generation evaluated using the variable charge loads at different Temperatures.