Oral PhD

CAFM study of Negative Bias Temperature Instability and Channel hot-carriers degradation in strained and non-strained MOSFETs

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This work addresses the impact of different electrical stresses, BTI (Bias Temperature Instability) and CHC (Channel Hot Carrier) stresses, on the nanoscale electrical properties of the MOSFET gate dielectric. First, thanks to its capability to investigate nanometer-sized regions, CAFM is shown to be powerful enough to evaluate the degradation induced in the different regions of the gate oxide along the channel. In particular, it is demonstrated that, while the BTI degradation is homogeneous, the CHC stress degradation, being higher close to the source (S) and the drain (D). Secondly, when comparing strained and non-strained channel devices, the results show that strained devices are more sensitive to CHC stress than non-strained ones.

1. Introduction

With the scaling of the MOSFET dimensions, the electric fields in the device increases, triggering different aging mechanisms, such as CHC, BTI and Dielectric Breakdown (BD) [1]. On the other hand, strain techniques have been presented as one way to enhance carrier mobility [2], though, the effects of CHC and BTI stresses can be enlarged [3]. In this work, the nanoscale electrical properties of the MOSFET gate dielectric are studied with CAFM after BTI and CHC stresses. Since very small areas can be analyzed with this technique, the effect of the stress in the different regions (along the channel) of the gate dielectric will be investigated. The impact of a CHC stress on strained MOSFETs will be also analyzed.

2. Experimental

p-MOSFETs (W=0.5µm, L=0.13, 0.5, 1 and 3µm) with a 1.4nm thick SiON layer as gate dielectric have been analyzed. In strained devices, SiGe at the S/D regions was deposited with a 15% Ge content. Some samples were subjected to CHC stress by applying -2.6V at drain and gate, and some other were subjected to Negative BTI stress (NBTI) by applying -2.6V at the gate, while the other terminals were grounded. After 200 sec electrical stresses, the top electrode of the MOSFETs were removed for the nanoscale electrical measurements.

3. Discussion

First, the nanoscale effect of NBTI and CHC stress on the gate oxide electrical properties of non-strained MOSFETs has been compared. Fig. 1a-1c show, respectively, examples of typical current maps obtained at 3.6V on (a) non-stressed, (b) NBTI and (c) CHC stressed MOSFETs (L= 1µm). The measurable gate area has been delimited by a dotted line. Fig. 1d shows the averaged current profiles obtained along the channel for the three devices. After the electrical stress, brighter areas, corresponding to larger currents, were observed (which were related to NBTI and CHC degradation) while mainly noise level was measured in the non-stressed MOSFET. Moreover, the distribution of the leaky sites over the gate region is different for the different stresses. In the NBTI stressed MOSFET, the current shows a homogenous distribution along the channel, while in the CHC stressed device, gate current is especially larger in the regions close to the source and drain, indicating a higher degradation (i.e, a larger defect generation) at these regions. The generated defects close to S and D can be attributed to NBTI and CHC degradation, respectively [4]. Table 1 (a), which shows the dispersion, σ, and average current, <I>, measured