Invited

P. Godignon[1], M. Wojtaszek[1], N. Mestres[2], G. Rius[3] and F. Perez-Murano[1]

Challenges in nano-patterning of epitaxial graphene grown on Silicon Carbide wafers

[1]Centro Nacional de Microelectrónica (CNM-CSIC), Campus UAB, Cerdanyola del Valles, Barcelona, Spain
[2]Instituto de Ciencias de Materiales de Barcelona (ICMAB-CSIC), Campus UAB, Cerdanyola, Spain
[3]Nagoya Institute of Technology, Gokiso, Showa, 466-8555 Nagoya, Japan

Currently, the most promising technique to produce graphene at wafer-scale for industrial purposes seems to be epitaxial growth either by chemical vapor deposition (CVD) on a metallic substrate or by heating a SiC substrate up to the graphitization temperature. In the first case, because the metallic film is electrically conducting, the graphene film needs to be transferred to an insulating substrate for applications based on electronic transport. In the second case, the graphene can be directly used on the insulating SiC surface. Silicon sublimation from the SiC causes a carbon rich surface that nucleates an epitaxial graphene layer. The graphene growth rate was found to depend on the specific polar SiC crystal face: graphene forms continuous layer on Si-face (Fig 1a), while under certain growth conditions, graphene flakes can be obtained on the C-face the surface (Fig 1b). In both case, resulting surface is composed of SiC steps with micrometer wide terraces (Fig 1a). It has been shown that the graphene grown on the terraces sidewall is of poor quality. Then, lithography processes must be aligned with the terraces. In the case of graphene flakes on C-Face, the flake must be localised and lithography must be done based on the flake position. As a consequence, most of lithography steps must be done using electron beam lithography. An alternative to this standard technique is to growth the graphene on pre-patterned wafers with a template. A material able to withstand high temperature must be used as mask such as AlN (Fig 1c) [1] or Si_3N_4. On the other hand, nanoribbons on SiC combine the high mobilities of graphene on SiC with a gap opening capability thanks to quantum confinement observed in nanoribbons. Typically, the gap energy separation between the sub-bands is inversely proportional to the ribbon width, as well as on the edges type of the ribbons. Ribbons obtained by plasma etching after ebeam lithography typically create rough edges that cause electron scatters and strong localization effects appear. As an alternative to ebeam lithography, Local Anodic Oxidation (LAO) has been tested to define nanoribbons [2-3], as Silicon Carbide can be oxidized forming a SiO_2 dielectric layer. An electrically isolated narrow ribbon of graphene can be drawn in such way. However, the best way to generate high performances nanoribbons on SiC is to use selective growth on crystal facets of SiC [4]. Besides the on-axis facets, SiC has other crystal facets with low crystal indies such as the SiC "sidewalls" that connect the terraces on the on-axis wafer surface. These low-index facets grouped as (110n) and (112n) have been used to selectively growth high performances graphene nanoribbons [4]. The facets are created by standard lithography and RIE etching. Then, special growth parameters can be found to get growth only on the facet, the nanoribbon width being defined by the etched sidewall depth.

References

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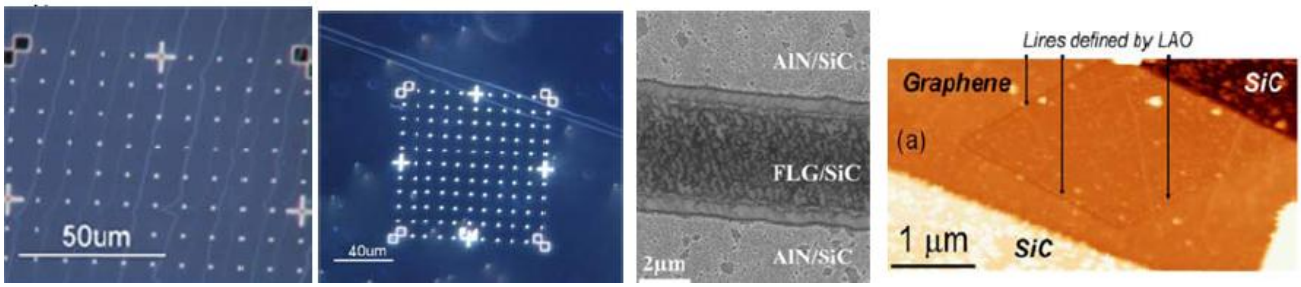

Figure 1. (a) graphene on SiC Si-face, (a) graphene on SiC C-face (c) graphene grown in AlN template, (d) graphene lithographed by LAO.