Sub-20 nm lift-off techniques without charged particle damage using Thermal Scanning Probe Lithography

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Abstract

Charged particle beams for the fabrication of devices comprising sensitive nanowires or 2D materials can lead to unwanted influence or damage of electronic properties of the device [1, 2]. Still, electron beam lithography (EBL) in combination with lift-off is the most commonly used method to fabricate prototypes of such devices.
Thermal Scanning Probe Lithography (t-SPL) is an alternative mask-less lithography technique with similar speed (up to 20 mm/s) and resolution (10 nm half-pitch) as EBL, but without charged particles involved [3, 4]. In this poster, we present two recently developed lift-off techniques for t-SPL that have enabled the creation of sub-20 nm Au, Pt and Ni structures and devices without the usage of high energy charged particle beams.

Thermal Scanning Probe Lithography (t-SPL) uses a heated silicon tip to locally decompose and evaporate a thermally responsive resist, usually PPA (polyphthalaldehye). PPA has been proven to be a suitable mask for pattern transfer into Si with sub-20 nm half-pitch using a hard mask stack [5].
A similar approach using a tri-layer stack was used to enable high resolution lift-off with metals. Figure 1a illustrates this lift-off method using a stack consisting of PPA, SiO_2 and PMMA. RIE is used to precisely define the undercut in PMMA for the subsequent lift-off. Figure 2 shows an InAs nanowire device, where top gate electrodes have been fabricated with 50 nm half-pitch using t-SPL and the lift-off method. The top gate electrodes have been overlaid on top of the InAs nanowire using the in-situ topography imaging method of t-SPL, which has been shown to be capable of sub-5 nm overlay accuracy [6]. No significant damage on the electrical properties of the InAs nanowire could be seen in such devices. Figure 3 and 4 show further examples with sub-20 nm features and gaps using t-SPL and this lift-off method.
The second lift-off method uses PMGI as under-layer and wet development to create the undercut (see Figure 1b). Parallel Pt lines with a half-pitch of 70 nm have been successfully fabricated (see Figure 5). We further demonstrate that smaller gaps can be created if the under-etched PPA is stable enough to remain free standing. The first test results demonstrate that it is possible to fabricate sub-20 nm metal gaps (see Figure 6).

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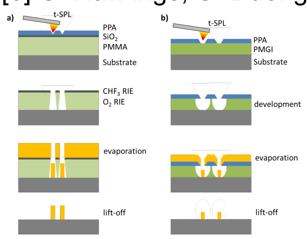

Figure 1

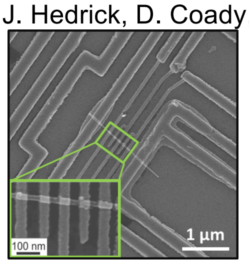

Figure 2

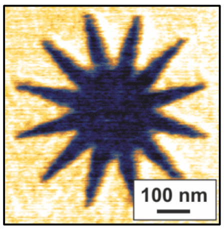

Figure 3

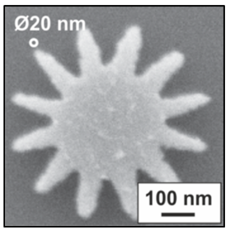

Figure 4

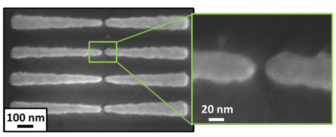

Figure 5

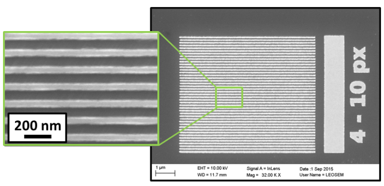

Figure 6

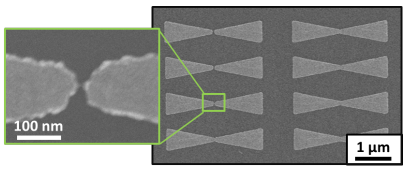

Figure 7